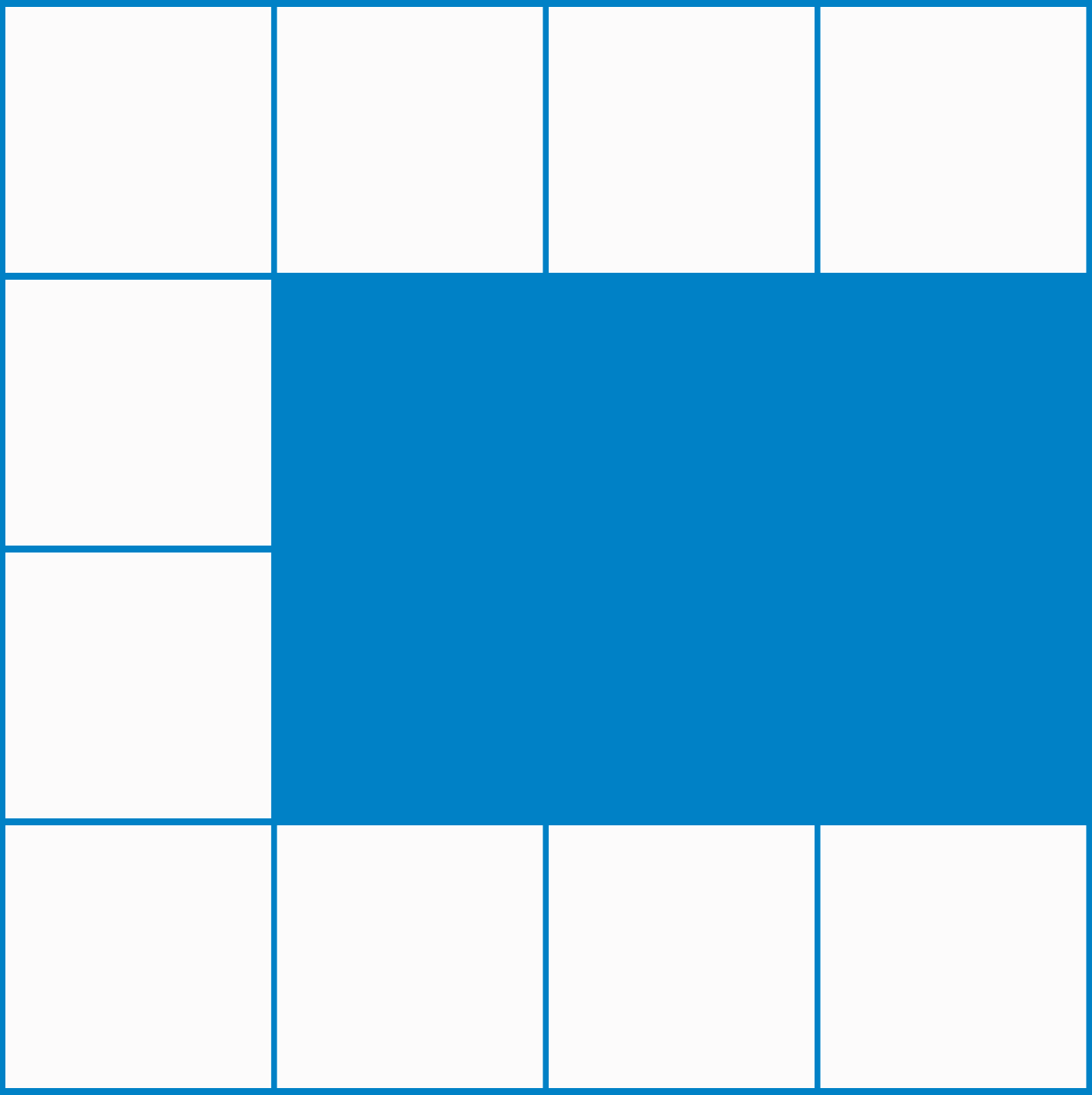
CRC Algorithm – IP-Core

PLC2

Ultrafast, Lightweight and Configurable CRC Implementation



The Cyclic Redundancy Check Algorithm

The Cyclic Redundancy Check (CRC) is a widely used error-detecting method designed to ensure data integrity during transmission and processing. Unfortunately, complex data calculations on wide buses often lead to significant performance loss. This VHDL IP core helps resolve this conflict: it provides exceptional speed in a highly generic and scalable CRC implementation, designed to cover virtually all CRC application scenarios with a single unified architecture. The same IP core can be configured and optimized to fit a broad range of requirements: A combination of exceptional sustained throughput in the multi-100-gigabit range and design flexibility within a fully vendor-independent architecture, ensuring maximum portability.

Key Features and Benefits



Ultra-high Performance: A fully pipelined architecture with flexible performance settings and the support for byte-enables ensures blockage-free streaming performance with consistent maximum throughput for ultra-high-speed data processing.



Linear resource utilization scaling: Predictable programmable logic utilization prevents unexpected resource shortages or overruns.



Data input flexibility: Integrates seamlessly into any IP block design or VHDL workflow delivering maximum flexibility and future-proof designs.



Vendor-independent architecture: Unified code portability across FPGA architectures eliminates vendor lock-in.



OSVVM testbench: Accelerates the critical phases of integration and release process, resulting in significant reductions in verification effort and time to market.

Applications

01 Ethernet IEEE Std. 802.3

Used for Ethernet Frame-Check-Sum (FCS) calculation from 1 GbE up to 100 GbE and beyond.

02 PCI Express

The IP core is applicable to PCI Express Link-CRC (LCRC) and End-to-End (ECRC) checksums.

03 Custom protocol implementations

Works with virtually any custom protocol implementation that needs high-bandwidth integrity checking.

04 Data integrity validation

End-to-End data integrity validation from source to destination for any type of content.

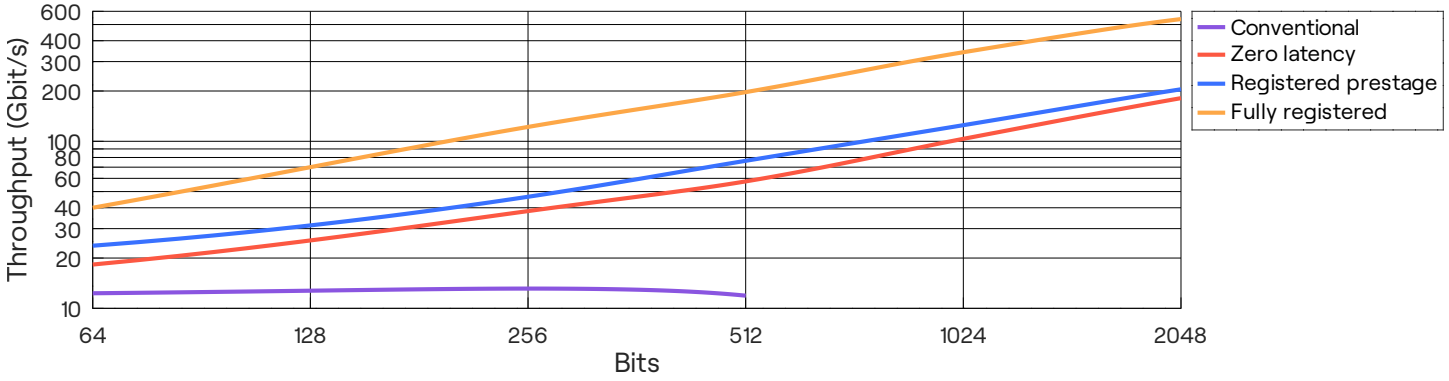
Specifications

- → Performance >400 Gbit/s fully pipelined and >150 Gbit/s in zero-delay mode
- → Configurable data input size from 32 bit to 2048 bit
- → Pipelined datapath for maximum throughput
- → Configurable CRC-polynomial, suitable for most protocols
- → Support for byte-enables
- → Flexible pipelining and performance settings
- → Linear ressources utilization scaling
- → Generic VHDL implementation without vendor-specific components or macros
- → Common CRC-output and data-input modifications (e.g. byte ordering, input-output inversion, etc.)
- → IP definition for block design or direct VHDL instantiation supported

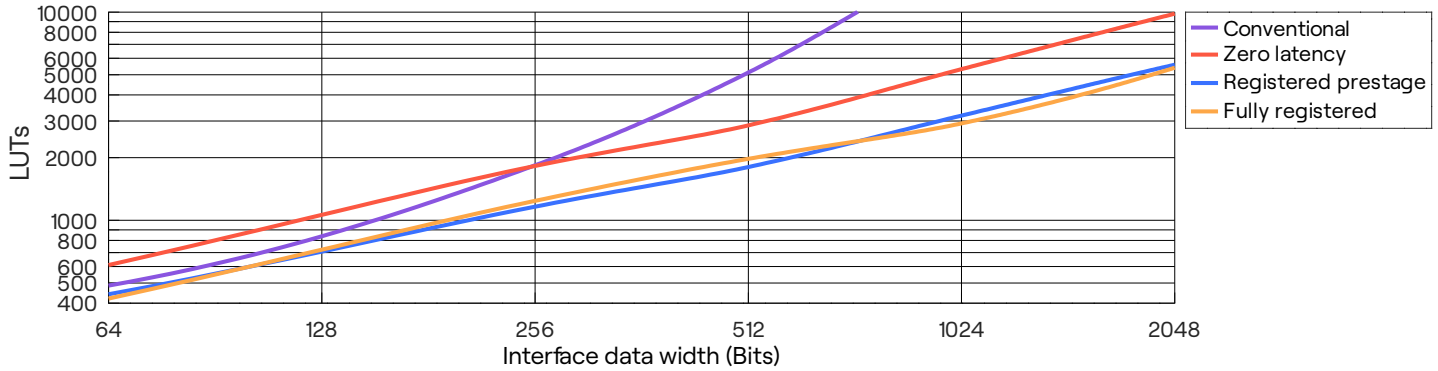
Core Specifics	
Supported device families	Vendor and device independent
Supported user interface	Custom interface (AXI4-Stream compatible)
Provided with Core	
Design files	Encrypted RTL
Example design	On request
Testbench	xSim (simple) and OSVVM testbench*
Constraints file	Not needed
Simulation model	VHDL 2008
Tested Design Flows	
Design entry	Vivado design suite (≥ 2018.3)
Simulators	xSim, Riviera-PRO™ and others
Synthesis	Vivado synthesis

Performance Metrics**

Data Throughput



Resource Utilization



* test cases on request

** tested with AMD Kintex™ 7 XC7K325T-2

PLC2

plc2 Design GmbH

Ersteiner Straße 19
79346 Endingen a. K.
Germany

+49 7642 92118 0

products@plc2.de | plc2.com
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