

# Training Calendar

# 2026

# Training Formats

## IH In-House

This format offers maximum flexibility for your technical training. Your team receives tailor-made courses that can be adapted precisely to your requirements in terms of format, content, duration, and location – efficiently, practically, and directly in the context of your own team.

[Read more](#)

## OL Online

Our PLC2 online training courses offer you the opportunity to acquire technical expertise in the desired and required depth. With the guidance of our instructors, you can perform the practical software exercises and projects directly on the hardware, ensuring a comprehensive and immersive learning experience.

## WE Webinar

The free 1-hour PLC2 webinars give participants a brief insight into a specific problem or topic. Our webinars shine with technical depth despite the limited time available. They are a good introduction to a certain topic.

## SE Seminar

Our free 1-day PLC2 seminars give developers, team leaders, and company management staff a comprehensive insight into the numerous possibilities surrounding the use of programmable technologies. Our competent instructors convey even difficult facts and contexts to you in an easily understandable way, while being present on-site. Individual questions and problems can be identified.

## ES Easy Start

Our 2-day Easy Start training courses were developed to make it easier for FPGA and MPSoC »newcomers« to get started in this field. We will train them in the use of the technology in general. This training series is also suitable for project managers, team leaders and group leaders.

The focus of this training format is on practical application with modern FPGAs/MPSoCs and less on the theoretical basis. The participants will be professionally guided by our experienced PLC2 experts to implement their own FPGA/MPSoC projects in order to take the first steps towards independent development of complex FPGAs/MPSoCs. Deeper theoretical foundations are taught in other training courses.

## WO Workshop

As the world's first and long-standing Authorized Training Provider (ATP) of Xilinx – today AMD, we always have access to brand-new technologies, methods, and development tools and work right at the forefront of the technological progress.

In our 2- and 3-day workshops, we share our knowledge with developers and train them in technical depth. During the training, the participant has the chance to consolidate and reinforce the knowledge imparted by our experts in practical exercises. The training portfolio ranges from workshops covering all HDL users to specific AMD technology training. The content focuses on methodologies for development and verification, the architecture of the latest building blocks, physical implementation, and the application of the highly complex development tools.

## PW Power Workshop

In the 5-day Power Workshops, our experts provide developers with particularly hands-on training in technical depth. Here, care is taken to ensure that the knowledge imparted is consolidated in the form of practical exercises.

Under the guidance and supervision of our competent trainers, the participants work intensively with laptops/PCs and, if required, with evaluation boards. Complex tasks are implemented, and the functionality is proven with the help of the simulation and the evaluation board.

The Power Workshops are suitable for all those who want to dive deeply into a topic and attach a lot of importance to practical relevance.

## LT Long Term Education

Demand more than basic training? Get ready for a deep, in-depth foundation in the FPGA or embedded field without delay. Our Long Term Education delivers the entire know-how on the latest state-of-the-art AMD FPGAs and SoCs.

In three 3-day blocks over three months, you receive full support, including boards, labs, software, telephone support, and a personal mentor. This ensures you can develop independently upon completion.

Get in touch with us to create your program.

# AMD Architecture

In today's competitive world of electronic engineering the difference is made at the system architectural level. Making the right choices at the start of your design makes the difference between mediocre versus excellent results. We at PLC2 can help you by providing training courses in the architecture area of the world's leading FPGAs from AMD. The workshops provide the foundation you need to get started with your FPGA development or to optimize your FPGA designs. Our classes are suited for both, FPGA newcomers and experienced developers.

 In-House
  Online
  Workshop
  Power Workshop

| Training                                        | Format                                                                              | Duration | January                                     | February | March    | April    | May       | June      | July     | August   | September | October   | November  | December | Fee                     |
|-------------------------------------------------|-------------------------------------------------------------------------------------|----------|---------------------------------------------|----------|----------|----------|-----------|-----------|----------|----------|-----------|-----------|-----------|----------|-------------------------|
| All courses available as In-House training      |    |          | all year on request at your chosen location |          |          |          |           |           |          |          |           |           |           |          | Calculated individually |
| Compact FPGA 7 Series                           |    | 2        | all year on request                         |          |          |          |           |           |          |          |           |           |           |          | € 1,900 / 20 TCs        |
| Compact FPGA 7 Series                           |    | 2        | all year on request                         |          |          |          |           |           |          |          |           |           |           |          | € 1,500 / 16 TCs        |
| Professional FPGA                               |    | 5        |                                             | 23–27, F |          |          | 18–22, FR |           | 13–17, F |          |           | 26–30, FR |           |          | € 3,500 / 40 TCs        |
| Professional FPGA                               |    | 5        |                                             | 23–27, O |          |          | 18–22, O  |           | 13–17, O |          |           | 26–30, O  |           |          | € 3,050 / 32 TCs        |
| <b>NEW</b> Compact Spartan UltraScale+          |    | 3        |                                             |          | 18–20, S |          |           |           | 22–24, F |          |           |           | 11–13, FR |          | € 2,500 / 30 TCs        |
| <b>NEW</b> Compact Spartan UltraScale+          |    | 3        |                                             |          | 18–20, O |          |           |           | 22–24, O |          |           |           | 11–13, O  |          | € 2,100 / 24 TCs        |
| Compact UltraScale/UltraScale+                  |    | 2        |                                             |          | 09–10, M |          |           | 15–16, FR |          |          | 17–18, F  |           | 11–12, S  |          | € 1,900 / 20 TCs        |
| Compact UltraScale/UltraScale+                  |    | 2        |                                             |          | 09–10, O |          |           | 15–16, O  |          |          | 17–18, O  |           | 11–12, O  |          | € 1,500 / 16 TCs        |
| Zynq UltraScale+ MPSoC for the System Architect |    | 2        |                                             |          | 09–10, S |          |           | 18–19, F  |          |          | 17–18, FR |           |           | 14–15, M | € 1,900 / 20 TCs        |
| Zynq UltraScale+ MPSoC for the System Architect |  | 2        |                                             |          | 09–10, O |          |           | 18–19, O  |          |          | 17–18, O  |           |           | 14–15, O | € 1,500 / 16 TCs        |
| Zynq 7000 SoC for the System Architect          |  | 2        | all year on request                         |          |          |          |           |           |          |          |           |           |           |          | € 1,900 / 20 TCs        |
| Zynq 7000 SoC for the System Architect          |  | 2        | all year on request                         |          |          |          |           |           |          |          |           |           |           |          | € 1,500 / 16 TCs        |
| Versal Adaptive SoC for the System Architect    |  | 2        | 19–20, FR                                   |          |          | 16–17, F |           |           |          | 13–14, S |           |           | 16–17, M  |          | € 1,900 / 20 TCs        |
| Versal Adaptive SoC for the System Architect    |  | 2        | 19–20, O                                    |          |          | 16–17, O |           |           |          | 13–14, O |           |           | 16–17, O  |          | € 1,500 / 16 TCs        |
| Essentials of Microprocessors                   |  | 1        | all year on request                         |          |          |          |           |           |          |          |           |           |           |          | € 900 / 10 TCs          |
| Essentials of Microprocessors                   |  | 1        | all year on request                         |          |          |          |           |           |          |          |           |           |           |          | € 700 / 8 TCs           |

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# Tools & Methodology <sup>1/3</sup>

The HDL-based development method simplifies the development cycle, but this requires the developer to have good knowledge of digital circuit design. It is not enough to know how to implement combinational and sequential circuits, it is very important to know how to implement your design in the FPGA architecture to maximize benefits in size, power, and performance.

The PLC2 training courses in the »Tools and Methodology« category help developers use and apply the development tools for these latest technologies.

IH In-House  
 OL Online  
 SE Seminar  
 ES Easy Start  
 WO Workshop  
 PW Power Workshop

| Training                                   | Format          | Duration | January                                     | February  | March    | April     | May       | June     | July      | August   | September | October   | November  | December  | Fee                         |
|--------------------------------------------|-----------------|----------|---------------------------------------------|-----------|----------|-----------|-----------|----------|-----------|----------|-----------|-----------|-----------|-----------|-----------------------------|
| All courses available as In-House training | <span>IH</span> |          | all year on request at your chosen location |           |          |           |           |          |           |          |           |           |           |           | Calculated individually     |
| Easy Start FPGA Vivado                     | <span>ES</span> | 2        |                                             |           | 11–12, M |           | 04–05, FR |          |           | 10–11, S |           |           | 23–24, F  |           | € 2,250* / 20 TCs + € 350** |
| Easy Start FPGA Vivado                     | <span>OL</span> | 2        |                                             |           | 11–12, O |           | 04–05, O  |          |           | 10–11, O |           |           | 23–24, O  |           | € 1,500 / 16 TCs            |
| FPGA Power Optimization                    | <span>WO</span> | 2        | all year on request                         |           |          |           |           |          |           |          |           |           |           |           | € 1,900 / 20 TCs            |
| FPGA Power Optimization                    | <span>OL</span> | 2        | all year on request                         |           |          |           |           |          |           |          |           |           |           |           | € 1,500 / 16 TCs            |
| Dynamic Function eXchange (DFX)            | <span>WO</span> | 2        | 29–30, M                                    |           |          | 27–28, F  |           |          | 09–10, S  |          |           | 12–13, FR |           |           | € 1,900 / 20 TCs            |
| Dynamic Function eXchange (DFX)            | <span>OL</span> | 2        | 29–30, O                                    |           |          | 27–28, O  |           |          | 09–10, O  |          |           | 12–13, O  |           |           | € 1,500 / 16 TCs            |
| FPGA Circuit Design Technique              | <span>SE</span> | 1        |                                             |           | 05, S    |           |           |          |           |          | 30, FR    |           |           |           | free of charge              |
| Compact FPGA Circuit Design Technique      | <span>WO</span> | 3        | 26–28, FR                                   |           |          |           | 11–13, F  |          |           | 12–14, S |           | 21–23, B  |           |           | € 2,500 / 30 TCs            |
| Compact FPGA Circuit Design Technique      | <span>OL</span> | 3        | 26–28, O                                    |           |          |           | 11–13, O  |          |           | 12–14, O |           | 21–23, O  |           |           | € 2,100 / 24 TCs            |
| Professional FPGA Circuit Design Technique | <span>PW</span> | 5        |                                             | 23–27, FR |          | 13–17, FR |           |          | 06–10, FR |          |           |           | 02–06, FR |           | € 3,500 / 40 TCs            |
| Professional FPGA Circuit Design Technique | <span>OL</span> | 5        |                                             | 23–27, O  |          | 13–17, O  |           |          | 06–10, O  |          |           |           | 02–06, O  |           | € 3,050 / 32 TCs            |
| Git for EDA Tool Flows                     | <span>WO</span> | 3        |                                             |           | 09–11, S |           |           | 01–03, M |           |          | 01–03, B  |           |           | 01–03, FR | € 2,500 / 30 TCs            |
| Git for EDA Tool Flows                     | <span>OL</span> | 3        |                                             |           | 09–11, O |           |           | 01–03, O |           |          | 01–03, O  |           |           | 01–03, O  | € 2,100 / 24 TCs            |
| Continuous Integration for EDA Tools       | <span>PW</span> | 5        |                                             | 23–27, S  |          |           | 04–08, FR |          | 27–31, F  |          |           | 05–09, B  |           |           | € 3,500 / 40 TCs            |
| Continuous Integration for EDA Tools       | <span>OL</span> | 5        |                                             | 23–27, O  |          |           | 04–08, O  |          | 27–31, O  |          |           | 05–09, O  |           |           | € 3,050 / 32 TCs            |

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\* including board  
 \*\* board

# Tools & Methodology <sup>2/3</sup>



In-House



Online



Workshop



Power Workshop

| Training                                             | Format | Duration | January                                     | February  | March     | April     | May      | June      | July     | August    | September | October   | November | December | Fee                     |
|------------------------------------------------------|--------|----------|---------------------------------------------|-----------|-----------|-----------|----------|-----------|----------|-----------|-----------|-----------|----------|----------|-------------------------|
| All courses available as In-House training           | IH     |          | all year on request at your chosen location |           |           |           |          |           |          |           |           |           |          |          | Calculated individually |
| Compact Vivado Design Suite Tool Flow                | WO     | 2        |                                             | 09–10, FR |           |           |          | 22–23, F  |          |           | 21–22, S  |           | 16–17, M |          | € 1,900 / 20 TCs        |
| Compact Vivado Design Suite Tool Flow                | OL     | 2        |                                             | 09–10, O  |           |           |          | 22–23, O  |          |           | 21–22, O  |           | 16–17, O |          | € 1,500 / 16 TCs        |
| Compact Timing Constraints and Analysis              | WO     | 3        |                                             | 11–13, FR |           |           |          | 24–26, FR |          |           | 23–25, S  |           | 18–20, M |          | € 2,500 / 30 TCs        |
| Compact Timing Constraints and Analysis              | OL     | 3        |                                             | 11–13, O  |           |           |          | 24–26, O  |          |           | 23–25, O  |           | 18–20, O |          | € 2,100 / 24 TCs        |
| Professional Vivado                                  | PW     | 5        |                                             |           | 23–27, FR |           |          |           | 27–31, F |           |           | 05–09, FR |          | 14–18, F | € 3,500 / 40 TCs        |
| Professional Vivado                                  | OL     | 5        |                                             |           | 23–27, O  |           |          |           | 27–31, O |           |           | 05–09, O  |          | 14–18, O | € 3,050 / 32 TCs        |
| Advanced Vivado                                      | WO     | 3        | 26–28, M                                    |           |           | 15–17, FR |          |           | 06–08, S |           |           | 14–16, F  |          |          | € 2,500 / 30 TCs        |
| Advanced Vivado                                      | OL     | 3        | 26–28, O                                    |           |           | 15–17, O  |          |           | 06–08, O |           |           | 14–16, O  |          |          | € 2,100 / 24 TCs        |
| Debugging Techniques Using the Vivado Logic Analyzer | WO     | 2        |                                             |           | 03–04, S  |           |          | 17–18, FR |          |           | 17–18, F  |           |          | 01–02, M | € 1,900 / 20 TCs        |
| Debugging Techniques Using the Vivado Logic Analyzer | OL     | 2        |                                             |           | 03–04, O  |           |          | 17–18, O  |          |           | 17–18, O  |           |          | 01–02, O | € 1,500 / 16 TCs        |
| Compact Vitis for the Software Designer              | WO     | 3        |                                             | 02–04, FR |           |           | 11–13, F |           |          |           | 07–09, B  |           |          | 16–18, M | € 2,500 / 30 TCs        |
| Compact Vitis for the Software Designer              | OL     | 3        |                                             | 02–04, O  |           |           | 11–13, O |           |          |           | 07–09, O  |           |          | 16–18, O | € 2,100 / 24 TCs        |
| Compact Vitis for Acceleration                       | WO     | 3        |                                             | 09–11, M  |           |           | 04–06, B |           |          | 17–19, FR |           |           | 25–27, F |          | € 2,500 / 30 TCs        |
| Compact Vitis for Acceleration                       | OL     | 3        |                                             | 09–11, O  |           |           | 04–06, O |           |          | 17–19, O  |           |           | 25–27, O |          | € 2,100 / 24 TCs        |
| Compact Vitis AI                                     | WO     | 3        |                                             |           | 18–20, F  |           |          | 01–03, FR |          |           | 01–03, S  |           | 10–12, B |          | € 2,500 / 30 TCs        |
| Compact Vitis AI                                     | OL     | 3        |                                             |           | 18–20, O  |           |          | 01–03, O  |          |           | 01–03, O  |           | 10–12, O |          | € 2,100 / 24 TCs        |

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# Tools & Methodology <sup>3/3</sup>

IH In-House  
 OL Online  
 WO Workshop  
 PW Power Workshop  
 LT Long Term Education

| Training                                            | Format          | Duration | January                                     | February | March                               | April                               | May                    | June     | July | August    | September                           | October                | November                            | December | Fee                     |
|-----------------------------------------------------|-----------------|----------|---------------------------------------------|----------|-------------------------------------|-------------------------------------|------------------------|----------|------|-----------|-------------------------------------|------------------------|-------------------------------------|----------|-------------------------|
| All courses available as In-House training          | <span>IH</span> |          | all year on request at your chosen location |          |                                     |                                     |                        |          |      |           |                                     |                        |                                     |          | Calculated individually |
| Professional Vitis                                  | <span>PW</span> | 5        |                                             |          | 16–20, F                            |                                     |                        | 15–19, S |      | 03–07, FR |                                     |                        | 09–13, B                            |          | € 3,500 / 40 TCs        |
| Professional Vitis                                  | <span>OL</span> | 5        |                                             |          | 16–20, O                            |                                     |                        | 15–19, O |      | 03–07, O  |                                     |                        | 09–13, O                            |          | € 3,050 / 32 TCs        |
| Scripting the AMD Hardware Design Flow Using Vivado | <span>WO</span> | 3        |                                             |          | 23–25, FR                           |                                     |                        | 01–03, M |      |           | 16–18, F                            |                        | 23–25, B                            |          | € 2,500 / 30 TCs        |
| Scripting the AMD Hardware Design Flow Using Vivado | <span>OL</span> | 3        |                                             |          | 23–25, O                            |                                     |                        | 01–03, O |      |           | 16–18, O                            |                        | 23–25, O                            |          | € 2,100 / 24 TCs        |
| Compact Edge AI Application Design Flow             | <span>WO</span> | 3        |                                             | 18–20, F |                                     |                                     | 27–29, FR              |          |      |           | 14–16, M                            |                        | 25–27, S                            |          | € 2,500 / 30 TCs        |
| Compact Edge AI Application Design Flow             | <span>OL</span> | 3        |                                             | 18–20, O |                                     |                                     | 27–29, O               |          |      |           | 14–16, O                            |                        | 25–27, O                            |          | € 2,100 / 24 TCs        |
| FPGA Designer (Long Term)                           | <span>LT</span> | 16       |                                             |          | 09–10, FR<br>16–17, FR<br>25–26, FR | 13–14, FR<br>20–21, FR<br>27–28, FR | 11–12, FR<br>20–21, FR |          |      |           | 15–16, FR<br>21–22, FR<br>28–29, FR | 05–06, FR<br>19–20, FR | 09–10, FR<br>18–19, FR<br>25–26, FR |          | € 9,200                 |

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# Programming Languages <sup>1/2</sup>

Familiarize yourself with the latest design methods to get the most out of your chosen technology. Learn the fundamentals and become an expert in HDL languages such as VHDL or System Verilog.

We offer a variety of workshops and training sessions to introduce you to System Verilog HDL and VHDL. You will learn the VHDL synthesis and simulation concept and understand how to use different synthesis or simulation constructs to design your FPGA.

IH In-House  
 OL Online  
 SE Seminar  
 WO Workshop  
 PW Power Workshop

| Training                                                  | Format          | Duration | January                                     | February  | March     | April | May       | June      | July      | August   | September | October   | November | December  | Fee                     |
|-----------------------------------------------------------|-----------------|----------|---------------------------------------------|-----------|-----------|-------|-----------|-----------|-----------|----------|-----------|-----------|----------|-----------|-------------------------|
| All courses available as In-House training                | <span>IH</span> |          | all year on request at your chosen location |           |           |       |           |           |           |          |           |           |          |           | Calculated individually |
| Circuit Synthesis with VHDL                               | <span>SE</span> | 1        |                                             |           |           | 22, F |           |           |           |          |           | 07, M     |          |           | free of charge          |
| Compact VHDL for Synthesis                                | <span>WO</span> | 3        |                                             |           | 16–18, FR |       |           | 15–17, F  |           |          | 21–23, S  |           | 23–25, M |           | € 2,500 / 30 TCs        |
| Compact VHDL for Synthesis                                | <span>OL</span> | 3        |                                             |           | 16–18, O  |       |           | 15–17, O  |           |          | 21–23, O  |           | 23–25, O |           | € 2,100 / 24 TCs        |
| Circuit Simulation with VHDL                              | <span>SE</span> | 1        |                                             |           |           |       | 06, FR    |           |           |          |           |           | 24, F    |           | free of charge          |
| Compact VHDL for Simulation                               | <span>WO</span> | 2        |                                             |           | 19–20, FR |       |           | 18–19, F  |           |          | 24–25, S  |           | 26–27, M |           | € 1,900 / 20 TCs        |
| Compact VHDL for Simulation                               | <span>OL</span> | 2        |                                             |           | 19–20, O  |       |           | 18–19, O  |           |          | 24–25, O  |           | 26–27, O |           | € 1,500 / 16 TCs        |
| Professional VHDL                                         | <span>PW</span> | 5        |                                             | 02–06, FR |           |       | 18–22, FR |           | 20–24, FR |          |           | 12–16, S  |          | 07–11, FR | € 3,500 / 40 TCs        |
| Professional VHDL                                         | <span>OL</span> | 5        |                                             | 02–06, O  |           |       | 18–22, O  |           | 20–24, O  |          |           | 12–16, O  |          | 07–11, O  | € 3,050 / 32 TCs        |
| Advanced VHDL                                             | <span>WO</span> | 3        |                                             |           | 16–18, S  |       |           |           | 13–15, F  |          |           | 19–21, FR |          | 14–16, M  | € 2,500 / 30 TCs        |
| Advanced VHDL                                             | <span>OL</span> | 3        |                                             |           | 16–18, O  |       |           |           | 13–15, O  |          |           | 19–21, O  |          | 14–16, O  | € 2,100 / 24 TCs        |
| Compact VHDL Testbenches and Verification with OSVVM      | <span>WO</span> | 3        |                                             |           | 02–04, S  |       | 27–29, FR |           |           | 04–06, B |           | 12–14, M  |          |           | € 2,500 / 30 TCs        |
| Compact VHDL Testbenches and Verification with OSVVM      | <span>OL</span> | 3        |                                             |           | 02–04, O  |       | 27–29, O  |           |           | 04–06, O |           | 12–14, O  |          |           | € 2,100 / 24 TCs        |
| Professional VHDL Testbenches and Verification with OSVVM | <span>PW</span> | 5        |                                             | 09–13, FR |           |       |           | 22–26, FR |           |          | 07–11, FR |           | 09–13, S |           | € 3,500 / 40 TCs        |
| Professional VHDL Testbenches and Verification with OSVVM | <span>OL</span> | 5        |                                             | 09–13, O  |           |       |           | 22–26, O  |           |          | 07–11, O  |           | 09–13, O |           | € 3,050 / 32 TCs        |

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# Programming Languages <sup>2/2</sup>



In-House



Online



Workshop



Power Workshop

| Training                                              | Format | Duration | January                                     | February | March    | April    | May | June      | July      | August | September | October  | November | December | Fee                     |
|-------------------------------------------------------|--------|----------|---------------------------------------------|----------|----------|----------|-----|-----------|-----------|--------|-----------|----------|----------|----------|-------------------------|
| All courses available as In-House training            | IH     |          | all year on request at your chosen location |          |          |          |     |           |           |        |           |          |          |          | Calculated individually |
| Compact System Verilog for Synthesis                  | WO     | 3        |                                             | 25–27, S |          | 27–29, F |     |           | 27–29, FR |        |           | 26–28, M |          |          | € 2,500 / 30 TCs        |
| Compact System Verilog for Synthesis                  | OL     | 3        |                                             | 25–27, O |          | 27–29, O |     |           | 27–29, O  |        |           | 26–28, O |          |          | € 2,100 / 24 TCs        |
| SystemVerilog – Advanced Verification for FPGA Design | WO     | 3        | all year on request                         |          |          |          |     |           |           |        |           |          |          |          | € 2,500 / 30 TCs        |
| SystemVerilog – Advanced Verification for FPGA Design | OL     | 3        | all year on request                         |          |          |          |     |           |           |        |           |          |          |          | € 2,100 / 24 TCs        |
| UVM Testbench Made Easy                               | WO     | 2        | all year on request                         |          |          |          |     |           |           |        |           |          |          |          | € 1,900 / 20 TCs        |
| UVM Testbench Made Easy                               | OL     | 2        | all year on request                         |          |          |          |     |           |           |        |           |          |          |          | € 1,500 / 16 TCs        |
| Compact Python for Embedded                           | WO     | 3        |                                             |          | 23–25, S |          |     | 15–17, FR |           |        | 21–23, F  |          | 23–25, B |          | € 2,500 / 30 TCs        |
| Compact Python for Embedded                           | OL     | 3        |                                             |          | 23–25, O |          |     | 15–17, O  |           |        | 21–23, O  |          | 23–25, O |          | € 2,100 / 24 TCs        |
| Professional Python for Embedded                      | PW     | 5        |                                             |          | 23–27, S |          |     | 15–19, FR |           |        | 21–25, F  |          | 23–27, B |          | € 3,500 / 40 TCs        |
| Professional Python for Embedded                      | OL     | 5        |                                             |          | 23–27, O |          |     | 15–19, O  |           |        | 21–25, O  |          | 23–27, O |          | € 3,050 / 32 TCs        |

# Embedded Development <sup>1/3</sup>

Are you a beginner in the embedded world or a very experienced embedded developer? We at PLC2 tailor our embedded classes to your level. Our workshops include everything you need to know on how to develop embedded solutions with AMD's wide range of SoCs. Understand the embedded design flow for the latest technologies from AMD including Versal adaptive SoC. There are software specific training topics on C/C++ as well as Linux and driver development under Linux.

IH In-House
 OL Online
 ES Easy Start
 WO Workshop
 PW Power Workshop

| Training                                                  | Format          | Duration | January                                     | February  | March     | April | May       | June     | July | August   | September | October  | November  | December  | Fee                         |
|-----------------------------------------------------------|-----------------|----------|---------------------------------------------|-----------|-----------|-------|-----------|----------|------|----------|-----------|----------|-----------|-----------|-----------------------------|
| All courses available as In-House training                | <span>IH</span> |          | all year on request at your chosen location |           |           |       |           |          |      |          |           |          |           |           | Calculated individually     |
| Easy Start Embedded for Zynq UltraScale+ MPSoC Systems    | <span>ES</span> | 2        |                                             |           | 11–12, S  |       |           | 18–19, F |      |          |           | 05–06, B |           | 03–04, FR | € 1,900 / 20 TCs            |
| Easy Start Embedded Flow                                  | <span>ES</span> | 2        |                                             |           | 25–26, FR |       |           | 22–23, F |      |          | 10–11, B  |          | 16–17, S  |           | € 2,250* / 20 TCs + € 350** |
| Easy Start ML Application Design Flow                     | <span>ES</span> | 2        |                                             | 05–06, FR |           |       |           | 08–09, F |      |          | 03–04, S  |          |           | 07–08, M  | € 1,900 / 20 TCs            |
| Compact Zynq UltraScale+ MPSoC for the Hardware Designer  | <span>WO</span> | 3        |                                             | 17–19, F  |           |       | 04–06, FR |          |      | 18–20, B |           |          | 02–04, M  |           | € 2,500 / 30 TCs            |
| Compact Zynq UltraScale+ MPSoC for the Hardware Designer  | <span>OL</span> | 3        |                                             | 17–19, O  |           |       | 04–06, O  |          |      | 18–20, O |           |          | 02–04, O  |           | € 2,100 / 24 TCs            |
| Advanced Zynq UltraScale+ MPSoC for the Hardware Designer | <span>WO</span> | 3        | all year on request                         |           |           |       |           |          |      |          |           |          |           |           | € 2,500 / 30 TCs            |
| Advanced Zynq UltraScale+ MPSoC for the Hardware Designer | <span>OL</span> | 3        | all year on request                         |           |           |       |           |          |      |          |           |          |           |           | € 2,100 / 24 TCs            |
| Compact Zynq UltraScale+ MPSoC for the Software Designer  | <span>WO</span> | 3        |                                             | 02–04, S  |           |       | 27–29, F  |          |      | 04–06, B |           |          | 11–13, FR |           | € 2,500 / 30 TCs            |
| Compact Zynq UltraScale+ MPSoC for the Software Designer  | <span>OL</span> | 3        |                                             | 02–04, O  |           |       | 27–29, O  |          |      | 04–06, O |           |          | 11–13, O  |           | € 2,100 / 24 TCs            |
| Advanced Zynq UltraScale+ MPSoC for the Software Designer | <span>WO</span> | 3        |                                             |           | 09–11, M  |       |           | 15–17, F |      |          | 28–30, FR |          |           | 01–03, S  | € 2,500 / 30 TCs            |
| Advanced Zynq UltraScale+ MPSoC for the Software Designer | <span>OL</span> | 3        |                                             |           | 09–11, O  |       |           | 15–17, O |      |          | 28–30, O  |          |           | 01–03, O  | € 2,100 / 24 TCs            |
| Professional Zynq UltraScale+ MPSoC                       | <span>PW</span> | 5        |                                             |           | 02–06, FR |       |           | 22–26, F |      |          | 07–11, FR |          |           | 07–11, F  | € 3,500 / 40 TCs            |
| Professional Zynq UltraScale+ MPSoC                       | <span>OL</span> | 5        |                                             |           | 02–06, O  |       |           | 22–26, O |      |          | 07–11, O  |          |           | 07–11, O  | € 3,050 / 32 TCs            |
| Easy Start Embedded for Zynq 7000 SoC Systems             | <span>ES</span> | 2        | all year on request                         |           |           |       |           |          |      |          |           |          |           |           | € 2,250* / 20 TCs + € 350** |
| Compact Zynq 7000 SoC for the Hardware Designer           | <span>WO</span> | 3        | all year on request                         |           |           |       |           |          |      |          |           |          |           |           | € 2,500 / 30 TCs            |
| Compact Zynq 7000 SoC for the Hardware Designer           | <span>OL</span> | 3        | all year on request                         |           |           |       |           |          |      |          |           |          |           |           | € 2,100 / 24 TCs            |

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\* including board  
 \*\* board

# Embedded Development <sup>2/3</sup>

IH In-House
 OL Online
 WO Workshop
 PW Power Workshop

| Training                                              | Format | Duration | January                                     | February | March    | April    | May      | June      | July      | August    | September | October  | November | December | Fee                     |
|-------------------------------------------------------|--------|----------|---------------------------------------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|----------|----------|----------|-------------------------|
| All courses available as In-House training            | IH     |          | all year on request at your chosen location |          |          |          |          |           |           |           |           |          |          |          | Calculated individually |
| Compact Zynq 7000 SoC for the Software Designer       | WO     | 3        | all year on request                         |          |          |          |          |           |           |           |           |          |          |          | € 2,500 / 30 TCs        |
| Compact Zynq 7000 SoC for the Software Designer       | OL     | 3        | all year on request                         |          |          |          |          |           |           |           |           |          |          |          | € 2,100 / 24 TCs        |
| Professional Zynq 7000 SoC                            | PW     | 5        | all year on request                         |          |          |          |          |           |           |           |           |          |          |          | € 3,500 / 40 TCs        |
| Professional Zynq 7000 SoC                            | OL     | 5        | all year on request                         |          |          |          |          |           |           |           |           |          |          |          | € 3,050 / 32 TCs        |
| Expert Zynq 7000 SoC                                  | PW     | 5        | all year on request                         |          |          |          |          |           |           |           |           |          |          |          | € 3,500 / 40 TCs        |
| Expert Zynq 7000 SoC                                  | OL     | 5        | all year on request                         |          |          |          |          |           |           |           |           |          |          |          | € 3,050 / 32 TCs        |
| Compact Versal Adaptive SoC for the Hardware Designer | WO     | 3        | 21–23, FR                                   |          |          | 13–15, F |          |           | 20–22, M  |           |           | 12–14, S |          |          | € 2,500 / 30 TCs        |
| Compact Versal Adaptive SoC for the Hardware Designer | OL     | 3        | 21–23, O                                    |          |          | 13–15, O |          |           | 20–22, O  |           |           | 12–14, O |          |          | € 2,100 / 24 TCs        |
| Compact Versal Adaptive SoC for the Software Designer | WO     | 3        |                                             | 25–27, S |          |          | 11–13, F |           |           | 24–26, FR |           | 07–09, B |          |          | € 2,500 / 30 TCs        |
| Compact Versal Adaptive SoC for the Software Designer | OL     | 3        |                                             | 25–27, O |          |          | 11–13, O |           |           | 24–26, O  |           | 07–09, O |          |          | € 2,100 / 24 TCs        |
| Professional Versal Adaptive SoC                      | PW     | 5        |                                             |          | 02–06, F |          |          | 22–26, FR |           |           | 21–25, S  |          | 02–06, M |          | € 3,500 / 40 TCs        |
| Professional Versal Adaptive SoC                      | OL     | 5        |                                             |          | 02–06, O |          |          | 22–26, O  |           |           | 21–25, O  |          | 02–06, O |          | € 3,050 / 32 TCs        |
| Advanced Versal Adaptive SoC AI Engine                | WO     | 3        |                                             |          | 11–13, S |          |          | 24–26, F  |           |           | 28–30, FR |          |          | 09–11, M | € 2,500 / 30 TCs        |
| Advanced Versal Adaptive SoC AI Engine                | OL     | 3        |                                             |          | 11–13, O |          |          | 24–26, O  |           |           | 28–30, O  |          |          | 09–11, O | € 2,100 / 24 TCs        |
| Expert Versal Adaptive SoC AI Engine                  | PW     | 5        | 26–30, S                                    |          |          | 20–24, F |          |           | 13–17, FR |           |           | 19–23, M |          |          | € 3,500 / 40 TCs        |
| Expert Versal Adaptive SoC AI Engine                  | OL     | 5        | 26–30, O                                    |          |          | 20–24, O |          |           | 13–17, O  |           |           | 19–23, O |          |          | € 3,050 / 32 TCs        |

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# Embedded Development <sup>3/3</sup>

IH In-House 
 OL Online 
 SE Seminar 
 ES Easy Start 
 WO Workshop 
 LT Long Term Education

| Training                                                              | Format          | Duration | January                                     | February  | March    | April    | May       | June      | July     | August   | September | October  | November  | December | Fee                     |
|-----------------------------------------------------------------------|-----------------|----------|---------------------------------------------|-----------|----------|----------|-----------|-----------|----------|----------|-----------|----------|-----------|----------|-------------------------|
| All courses available as In-House training                            | <span>IH</span> |          | all year on request at your chosen location |           |          |          |           |           |          |          |           |          |           |          | Calculated individually |
| Compact Edge IoT                                                      | <span>WO</span> | 3        |                                             |           | 02–04, S |          |           | 01–03, FR |          |          | 07–09, B  |          |           | 01–03, F | € 2,500 / 30 TCs        |
| Compact Edge IoT                                                      | <span>OL</span> | 3        |                                             |           | 02–04, O |          |           | 01–03, O  |          |          | 07–09, O  |          |           | 01–03, O | € 2,100 / 24 TCs        |
| Compact MicroBlaze V System Design                                    | <span>WO</span> | 3        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 2,500 / 30 TCs        |
| Compact MicroBlaze V System Design                                    | <span>OL</span> | 3        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 2,100 / 24 TCs        |
| Developing Multimedia Solutions with the VCU and GStreamer            | <span>WO</span> | 2        |                                             | 05–06, S  |          |          | 07–08, FR |           | 20–21, F |          |           | 20–21, B |           |          | € 1,900 / 20 TCs        |
| Developing Multimedia Solutions with the VCU and GStreamer            | <span>OL</span> | 2        |                                             | 05–06, O  |          |          | 07–08, O  |           | 20–21, O |          |           | 20–21, O |           |          | € 1,500 / 16 TCs        |
| Compact Embedded Linux                                                | <span>WO</span> | 3        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 2,500 / 30 TCs        |
| Compact Embedded Linux                                                | <span>OL</span> | 3        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 2,100 / 24 TCs        |
| Embedded Linux Driver Development                                     | <span>WO</span> | 3        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 2,500 / 30 TCs        |
| Embedded Linux Driver Development                                     | <span>OL</span> | 3        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 2,100 / 24 TCs        |
| <b>NEW</b> Easy Start AMD Embedded Linux                              | <span>ES</span> | 2        |                                             |           |          | 29–30, F |           |           |          | 24–25, M |           |          | 09–10, FR |          | € 1,900 / 20 TCs        |
| Embedded Design with PetaLinux Tools                                  | <span>WO</span> | 2        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 1,900 / 20 TCs        |
| Embedded Design with PetaLinux Tools                                  | <span>OL</span> | 2        | all year on request                         |           |          |          |           |           |          |          |           |          |           |          | € 1,500 / 16 TCs        |
| Yocto Embedded Linux Development                                      | <span>WO</span> | 2        |                                             | 24–25, FR |          |          |           | 01–02, M  |          |          | 14–15, F  |          | 09–10, FR |          | € 1,900 / 20 TCs        |
| <b>NEW</b> Embedded Linux Development - PetaLinux, Yocto and EDF Flow | <span>WO</span> | 3        |                                             |           |          |          |           |           | 22–24, F |          |           |          | 18–20, S  |          | € 2,500 / 30 TCs        |

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# Embedded Development 3/3

IH In-House   OL Online   SE Seminar   ES Easy Start   WO Workshop   LT Long Term Education

| Training                                   | Format          | Duration | January                                     | February | March | April                               | May                    | June                                | July | August | September | October                             | November                            | December               | Fee                         |
|--------------------------------------------|-----------------|----------|---------------------------------------------|----------|-------|-------------------------------------|------------------------|-------------------------------------|------|--------|-----------|-------------------------------------|-------------------------------------|------------------------|-----------------------------|
| All courses available as In-House training | <span>IH</span> |          | all year on request at your chosen location |          |       |                                     |                        |                                     |      |        |           |                                     |                                     |                        | Calculated individually     |
| Easy Start Kria for Vision Development     | <span>ES</span> | 2        |                                             | 19–20, F |       |                                     | 26–27, S               |                                     |      |        | 01–02, FR |                                     | 26–27, B                            |                        | € 2,250* / 20 TCs + € 350** |
| Kria for the Software Developer            | <span>SE</span> | 1        | all year on request                         |          |       |                                     |                        |                                     |      |        |           |                                     |                                     |                        | free of charge              |
| Embedded Designer (Long Term)              | <span>LT</span> | 16       |                                             |          |       | 15–16, FR<br>22–23, FR<br>29–30, FR | 07–08, FR<br>18–19, FR | 01–02, FR<br>16–17, FR<br>24–25, FR |      |        |           | 07–08, FR<br>14–15, FR<br>27–28, FR | 04–05, FR<br>16–17, FR<br>23–24, FR | 01–02, FR<br>09–10, FR | € 9,200                     |

# DSP & Image Processing

IH In-House
 OL Online
 WO Workshop
 PW Power Workshop

With their inherent flexibility, AMD FPGAs and SoCs are ideal for high-performance or multi-channel digital signal processing (DSP) applications that can take advantage of hardware parallelism. AMD FPGAs and SoCs combine this processing bandwidth with comprehensive solutions, including easy-to-use design tools for hardware designers, software developers, and system architects. We at PLC2 will teach you how to get the maximum out of these FPGAs and SoCs using Vitis Model Composer in interaction with Matlab Simulink. Additionally, you will learn how to develop HDL-based DSP functions.

| Training                                                 | Format          | Duration | January                                     | February | March | April | May      | June     | July | August    | September | October | November | December | Fee                     |
|----------------------------------------------------------|-----------------|----------|---------------------------------------------|----------|-------|-------|----------|----------|------|-----------|-----------|---------|----------|----------|-------------------------|
| All courses available as In-House training               | <span>IH</span> |          | all year on request at your chosen location |          |       |       |          |          |      |           |           |         |          |          | Calculated individually |
| Compact Vitis HLS                                        | <span>WO</span> | 3        |                                             | 18–20, F |       |       | 20–22, M |          |      | 10–12, FR |           |         | 18–20, S |          | € 2,500 / 30 TCs        |
| Compact Vitis HLS                                        | <span>OL</span> | 3        |                                             | 18–20, O |       |       | 20–22, O |          |      | 10–12, O  |           |         | 18–20, O |          | € 2,100 / 24 TCs        |
| Compact DSP Design for FPGAs Using Vitis Model Composer  | <span>WO</span> | 3        |                                             | 09–11, M |       |       |          | 22–24, F |      |           | 21–23, FR |         |          | 14–16, B | € 2,500 / 30 TCs        |
| Compact DSP Design for FPGAs Using Vitis Model Composer  | <span>OL</span> | 3        |                                             | 09–11, O |       |       |          | 22–24, O |      |           | 21–23, O  |         |          | 14–16, O | € 2,100 / 24 TCs        |
| Compact DSP Design for Versal Using Vitis Model Composer | <span>WO</span> | 3        | all year on request                         |          |       |       |          |          |      |           |           |         |          |          | € 2,500 / 30 TCs        |
| Compact DSP Design for Versal Using Vitis Model Composer | <span>OL</span> | 3        | all year on request                         |          |       |       |          |          |      |           |           |         |          |          | € 2,100 / 24 TCs        |
| Professional DSP Design Using Vitis Model Composer       | <span>PW</span> | 5        |                                             | 09–13, M |       |       |          | 22–26, F |      |           | 21–25, FR |         |          | 14–18, B | € 3,500 / 40 TCs        |
| Professional DSP Design Using Vitis Model Composer       | <span>OL</span> | 5        |                                             | 09–13, O |       |       |          | 22–26, O |      |           | 21–25, O  |         |          | 14–18, O | € 3,050 / 32 TCs        |

# FPGA Connectivity & Protocols

How do you keep up with the edge network emerging applications that are redefining hardware requirements for electronic designers? Are you designing the next generation AI for IoT, embedded vision, hardware security, 5G communication, or industrial/automotive automation for your company? Then PLC2 can teach you how the state-of-art AMD products can be used in your application for processing and bridging needs including high bandwidth sensor and display interfaces, video processing and machine learning inferencing.

IH In-House
 OL Online
 WO Workshop

| Training                                              | Format | Duration | January                                     | February | March     | April | May       | June     | July | August | September | October  | November | December | Fee                     |
|-------------------------------------------------------|--------|----------|---------------------------------------------|----------|-----------|-------|-----------|----------|------|--------|-----------|----------|----------|----------|-------------------------|
| All courses available as In-House training            | IH     |          | all year on request at your chosen location |          |           |       |           |          |      |        |           |          |          |          | Calculated individually |
| AXI Interface Technology                              | WO     | 2        |                                             |          | 23–24, FR |       |           | 18–19, F |      |        | 10–11, B  |          | 02–03, M |          | € 1,900 / 20 TCs        |
| AXI Interface Technology                              | OL     | 2        |                                             |          | 23–24, O  |       |           | 18–19, O |      |        | 10–11, O  |          | 02–03, O |          | € 1,500 / 16 TCs        |
| Compact Zynq UltraScale+ RFSoc                        | WO     | 3        |                                             | 02–04, B |           |       | 18–20, FR |          |      |        | 28–30, FR |          |          | 07–09, M | € 2,500 / 30 TCs        |
| Compact UltraScale: High-Speed Memory Interfacing     | WO     | 3        | all year on request                         |          |           |       |           |          |      |        |           |          |          |          | € 2,500 / 30 TCs        |
| Compact UltraScale: High-Speed Memory Interfacing     | OL     | 3        | all year on request                         |          |           |       |           |          |      |        |           |          |          |          | € 2,100 / 24 TCs        |
| Compact UltraScale: Serial Transceivers               | WO     | 3        |                                             |          | 16–18, M  |       |           | 24–26, B |      |        | 14–16, F  |          |          |          | € 2,500 / 30 TCs        |
| Compact UltraScale: Serial Transceivers               | OL     | 3        |                                             |          | 16–18, O  |       |           | 24–26, O |      |        | 14–16, O  |          |          |          | € 2,100 / 24 TCs        |
| Designing with Ethernet MAC Controllers               | WO     | 2        |                                             | 19–20, F |           |       | 28–29, S  |          |      |        | 03–04, FR |          | 05–06, M |          | € 1,900 / 20 TCs        |
| Designing with Ethernet MAC Controllers               | OL     | 2        |                                             | 19–20, O |           |       | 28–29, O  |          |      |        | 03–04, O  |          | 05–06, O |          | € 1,500 / 16 TCs        |
| Compact UltraScale: Integrated PCI Express System     | WO     | 3        |                                             | 23–25, S |           |       | 04–06, FR |          |      |        | 01–03, M  |          |          | 01–03, B | € 2,500 / 30 TCs        |
| Compact Versal Adaptive SoC: PCI Express Systems      | WO     | 2        |                                             |          | 19–20, M  |       |           | 22–23, B |      |        |           | 12–13, S |          |          | € 1,900 / 20 TCs        |
| Compact UltraScale: Board Design and Signal Integrity | WO     | 3        | all year on request                         |          |           |       |           |          |      |        |           |          |          |          | € 2,500 / 30 TCs        |
| Compact UltraScale: Board Design and Signal Integrity | OL     | 3        | all year on request                         |          |           |       |           |          |      |        |           |          |          |          | € 2,100 / 24 TCs        |
| Compact Versal Adaptive SoC: Power and Board Design   | WO     | 3        | all year on request                         |          |           |       |           |          |      |        |           |          |          |          | € 2,500 / 30 TCs        |
| Compact Versal Adaptive SoC: Power and Board Design   | OL     | 3        | all year on request                         |          |           |       |           |          |      |        |           |          |          |          | € 2,100 / 24 TCs        |

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