

| Applicable Technologies | Requirements  | Contact  |
|-------------------------|---|--|
| All FPGA technologies   | Knowledge in digital design development using VHDL        | Michael Schwarz<br>P. +49 7664 91313-15<br>E. info@plc2.de |
| Fee (net per person)    | Inclusive   | Duration   |
| <b>WO</b> € 300         | Training material<br><br>Beverages during breaks<br>Lunch | 1 day  |

## Workshop

Based on our experience from many years of VHDL training and consultancy work, engineers across Germany have a diverse skillset and understanding of VHDL. This highly interactive class wants to equalize the expertise, fill the knowledge gaps and discuss about old or maybe unknown VHDL features, which almost nobody uses due to missing tool support in the past.

This 1-day event mixes theory like VHDL types, with practical uses cases for big designs. We will discover VHDL as a powerful and modern hardware description language from bit-level synthesis up to system level testbenches. Of course, we will dive into VHDL-2019 features supported by state-of-the-art synthesis tools to increase engineers' productivity.

## Agenda

- 01. Basics - PLC2
  - Hardware Description Language (HDL) programming principles
  - Modern VHDL coding style.
  - VHDL's static type system
  - What signals to initialize (and what not)
  - VHDL's delay mechanisms (inertial vs. transport)
  - VHDL's delta cycles explained
  - Using physical types, such as TIME and FREQUENCY in synthesis
  - Unconstrained record and array types
  - Views (VHDL-2019 interfaces)
  - Design hierarchy: instantiations and VHDL-2008 generate blocks
  - VHDL's internal transformation rules
- 02. VHDL-2008 - PLC2
  - VHDL-2008 external names
  - VHDL-2008 protected types
  - Finite State Machines (FSMs)
  - Coupling of multiple FSMs
  - Debugging techniques
  - AXI4-Lite register interfaces, modes
  - Memory mapped and streaming bus
- 03. VHDL-2009 - PLC2
  - VHDL-2019 Conditional analysis
  - VHDL-2019 New APIs
    - Date
    - Time
    - File I/O, Directories
    - Environment variables
  - New and usable VHDL-2019 features
    - 64-bit integers
    - Function return sizes
    - Range records
    - New attributes
    - Incomplete types
    - Anonymous types
- 04. OSVVM - PLC2
  - OSVVM's AXI4 verification components
  - Regression testing, reporting, and CI integration with OSVVM
- 05. Sigasi Visual HDL - Sigasi
  - Introduction to Sigasi Visual HDL (SVH) SVH walkthrough
  - VHDL-2019 support in SVH
  - Enforcing good practices with SVH
  - »Vibe« coding with SVH

- Complimentary meet-up with open discussion
- Open-source HDL tooling
  - Open-source VHDL simulators
  - Open-source verification frameworks