FPGA Conference EUROPE

Program 2024

3 Days – 10 Thematic Focus Tracks – 100 Percent Knowhow

organized by ELEKTRONIK PRAXIS PLC2

Tuesday, July 2

8:45 - 9:00 am — **Welcome Session: Stefan Krassin | PLC2**

	Application	AI / ML	Language / Debug / Verification	Embedded	Tools & Methodologies	Tutorials
9:00 am - 10:30 am	Dr. Jörg Pospiech - AVT GmbH Ilmenau **Fast data transmission with Artix UltraScale+ via various interfaces** (40 min)	Alexander Flick - PLC2 **Vitis AI based ML Inference Applications** (40 min)	Marco Smutek - Arrow Central Europe GmbH **AI generated VHDL code – Fit for practice?** (40 min)	Konstantin Dobrosolets - Intel Deutschland GmbH **altera Agilex® 5 FPGAs for Video Solutions** (40 min)	Baruch Mitsengendler - The MathWorks GmbH **FPGA Verification as Part of Model-Based Design** (40 min)	Nikolai Krassin - PLC2 **Easy Start FPGA Vivado Part 1: Introduction to the FPGA Development Process** (90 min)
	Alexander Daum & Matthias Kern - FH Oberösterreich Studienbetriebs GmbH **100GbE from FPGA to Disk** (40 min)	Marco Höfle - Avnet EMG AG **AI/ML for Dummies: Designing a hand written number recognition model for an AMD Zynq™ UltraScale+™ platform** (40 min)	Jim Lewis - SynthWorks Design Inc **The Things I Hate about VHDL** (40 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Unlocking Efficiency: Practical Image Processing with AMD Vitis™** (40 min)	Tom Richter - The MathWorks GmbH **Linear Algebra on FPGA - From Theory to Implementation** (40 min)	
10:30 - 11:15 am	**Coffee break**					
11:15 am - 12:45 pm	Umran Yungucu - Bull Technologies **Reed-Solomon(528,514) Encoder-Decoder Design on FPGA for Low Latency and High Throughput Requirements** (40 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Mastering Adaptable AI: A Deep Dive into AMD Vitis™ AI and Beyond** (40 min)	Davide Cieri - Max Planck Institute for Physics **Hog (HDL-on-git): handling HDL repositories with git** (40 min)	David Kirchner - World of FPGA **Video Streaming with Zynq SoC: A Hybrid ARM-FPGA Approach** (40 min)	Dimitri Hamidi - The MathWorks GmbH **Automating Frame-to-Sample Algorithms Conversion for Vendor-Independent FPGA Implementation** (40 min)	Nikolai Krassin - PLC2 **Easy Start FPGA Vivado Part 2: FPGA Design Techniques** (90 min)
	Tomas Hudson - Monolithic Power Systems GmbH **Exploring Efficient FPGA Power Delivery: Multiphase Converters & Integrated Modules** (40 min)	Jerry Armao - AMD **Polyphase Channelizer Design for AI Engine** (40 min)	Dr. Hartmut Schorrig - Vishia **Objectoriented FPGA-Hardwaredesigns in Java** (40 min)	Patrice Brossard & Francisco Perez - Future Electronics S.A. **Optimizing power efficiency in Embedded Vision Systems** (40 min)	Ernst Wehlage - PLC2 **Performing H/W and S/W Co-Simulation using Vitis Model Composer** (40 min)	
12:45 - 1:30 pm	**Lunch break**					
1:30 - 2:00 pm	**KEYNOTE: From FPGAs to Heterogeneous Adaptive SoCs — And the Evolving Developer Experience | Michael Hutchison - AMD**					
2:00 - 2:15 pm	**Short break**					
2:15 pm - 3:45 pm	Tomas Hudson - Monolithic Power Systems GmbH & Udo Blaga - Avnet Silica **Simplifying Power Design for High-End AMD Xilinx FPGAs: Embracing Integrated Power Modules** (40 min)	Jens Stapelfeldt - AMD **AMD AI Stack and Opensource tool support** (90 min)	Markus Leiter - P2L2 **OSVVM, Cocotb, VUnit, UVVM, GHDL, NVC – Which Open-Source Tool Should I Use?** (40 min)	Anton Fogel & Mathias Sandner - Lauterbach GmbH **Improving the Bugfixing of Heterogeneous Multicore Hard- and Softcore Implementations in FPGA SoCs** (40 min)	Salma Hamdoun - Arrow Central Europe GmbH **Open-Source FPGA Tools and Frameworks** (40 min)	Nikolai Krassin - PLC2 **Easy Start FPGA Vivado Part 3: VHDL Synthesis and Simulation** (90 min)
	Leonardo Di Carlo - Microchip Technology GmbH **Benefits of low-power devices at the intelligent edge, a case study** (40 min)		Espen Tallaksen - EmLogic AS **Making a really advanced, but simple-to-understand FPGA testbench for complex DUTs** (40 min)	Ernst Wehlage - PLC2 **Inter-Processor Communication and Open AMP** (40 min)	Prof. Dirk Koch - Heidelberg University **All FPGAs are equal, but some FPGAs are more equal** (40 min)	
3:45 - 4:30 pm	**Coffee break**					
4:30 pm - 6:00 pm	Gordan Galic - Xylon d.o.o. **Configurable HDR ISP Pipeline with the RGB-IR Image Processing Capabilities** (40 min)	Jens Stapelfeldt - AMD **Adaptive SoC platform for Automotive AI applications** (90 min)	Jim Lewis - SynthWorks Design Inc **Why Should Our Team be Using VHDL+OSVVM for verification?** (40 min)	Stefan Garcia - Intel Deutschland GmbH **altera Agilex® 5 FPGA Hardened Processor Subsystem (HPS)** (40 min)	Alexander Wirthmueller - MPSI Technologies GmbH **Vendor-agnostic probing of FPGA designs for efficient run-time debugging** (40 min)	Nikolai Krassin - PLC2 **Easy Start FPGA Vivado Part 4: VHDL Finite State Machines** (90 min)
	Andreas Schuler - Missing Link Electronics GmbH **FPGA Based 400GBit/s Data Recorder - Insight into different pitfalls and design choices** (40 min)		Sonja Schoissengaier - FH Oberösterreich Studienbetriebs GmbH **Supporting VHDL in Visual Studio Code** (40 min)	Thomas Zerrer - Smartlogic GmbH **Designing Co-Processor applications with PCI-Express** (40 min)	Hans-Jürgen Schwender - TRIAS Mikroelektronik GmbH **Introducing Sequential Logic Equivalence Checking (SLEC)** (40 min)	
from 7:00 pm	**Evening Event @ Motorworld Inn in Munich**					

FPGA Conference EUROPE

Program 2024

3 Days – 10 Thematic Focus Tracks – 100 Percent Knowhow

organized by ELEKTRONIK PRAXIS PLC2

Wednesday, July 3

	Application	Basics	AI / ML	Architecture	Safety & Security / Board Design & Connectivity	Tutorial
9:00 am - 10:30 am	Andreas Kick - Siemens AG **FPGA Application to Control an Optical Scan Head** (40 min)	Ernst Wehlage - PLC2 **AMD Design Flows and the Build Formats** (90 min)	Dr. Aurang Zaib - Microchip Technology GmbH **Application-oriented Flow for Machine Learning on Microchip FPGAs** (40 min)	Thomas Siebert - Intel Deutschland GmbH **altera Agilex® 5 FPGA External Memory Interfaces (EMIF)** (40 min)	Oren Hollander - HandsOn Training **Modern FPGAs Security Features** (40 min)	Espen Tallaksen - EmLogic AS **Verifying a simple DUT (FPGA or module) from scratch with basic verification – for beginners** (90 min)
	Patrick Lehmann - PLC2 **Continuous Documentation for HDL Engineers** (40 min)			Thomas Siebert - Intel Deutschland GmbH **Implementing High-Speed Serial Interfaces in altera Agilex® 5 FPGAs** (40 min)	Shivani Saravanan - Intel Deutschland GmbH **altera Agilex® 5 FPGA Advanced Security Features** (40 min)	
10:30 - 11:15 am	**Coffee break**					
11:15 am - 12:45 pm	Dr. Dmitry Eliseev - RWTH Aachen University **An open-source IP-Core to implement a 1GSPS multi-channel ADC within your FPGA** (40 min)	Nikolai Krassin - PLC2 **Introduction to AMD FPGA Architecture** (90 min)	Christian Färber - Intel Deutschland GmbH **Introduction to Intel® FPGA AI Suite for altera® FPGAs** (40 min)	Oren Hollander - HandsOn Training **Cortex-A and Nios V (RISC-V) in Agilex 5** (40 min)	Martin Kellermann - Microchip Technology GmbH & Jens Michaelsen - Avnet Silica **Embedded system design: know it, know someone, or get to know.** (40 min)	Espen Tallaksen - EmLogic AS **Verifying a complex DUT in a simple way from scratch** (90 min)
	Jorge André Gastmaier Marques - Analog Devices Inc. **Open Source I3C Controller, a full stack solution** (40 min)		Alexey Lopich - Intel Corporation **Camera Pipeline at the Edge: Designing End-to-End Image Signal Processing and AI on FPGAs** (40 min)	Dr. Aurang Zaib - Microchip Technology GmbH **Embedded Linux Support for Hardware Software Interaction in Microchip FPGA SoCs** (40 min)	Harald Friedrich - NewTec GmbH **FPGAs in safety critical applications – key considerations, challenges and opportunities in automotive and industrial designs** (40 min)	
12:45 - 1:30 pm	**Lunch break**					
1:30 - 2:00 pm	**KEYNOTE: Intelligent edge – empowering innovation by making open-source RISC-V development hardware affordable and accessible | Ted Speers - Microchip Technology Inc.**					
2:00 - 2:15 pm	**Short break**					
2:15 pm - 3:45 pm	Dirk van den Heuvel - Topic Embedded Systems **What challenges do we encounter while working at the edge of technology** (40 min)	Kamil Rudnicki - Brightelligence sp. z o.o. **Overview of highly efficient design techniques for FPGA firmware development flow** (40 min)	Martin Kellermann - Microchip Technology GmbH & Jens Michaelsen - Avnet Silica **Machine learning: flexible hardware to ease software design** (90 min)	Alexander Flick - PLC2 **Versal™ Adaptive SoC Architecture and Tool Flow** (40 min)	Lukáš Kekely - BrnoLogic **Challenges of FPGA-Based SmartNICs for 400 Gbps+** (40 min)	Christiaan Baaij - QBayLogic B.V. **FPGA design in a functional programming language** (90 min)
	Prof. Dr. Markus Pfaff - FH Oberösterreich Studienbetriebs GmbH - P2L2 GmbH **RTL on a Higher Level: Introducing the Hierarchical FSMD** (40 min)	Harald Flügel - Arrow Central Europe GmbH **LUT, logic element, logic cell, system logic cell – Comparing FPGA Complexity** (40 min)		Alexander Flick - PLC2 **Edge IOT Applications with Versal Adaptive SoCs** (40 min)	Dr. Thomas Kirchner - Keysight Technologies Deutschland GmbH **Transmitter Output Signal Integrity Tests for 400G and 800G Pluggable Transceivers Modules and Hosts** (40 min)	
3:45 - 4:30 pm	**Coffee break**					
4:30 pm - 6:00 pm	Martin Kellermann - Microchip Technology GmbH **Full steam ahead: power-efficient communication solutions** (40 min)	Patrick Lehmann - PLC2 **Constraining Multiple Clock Domains** (90 min)	Joachim Müller - Efinix Inc. **RISC-V with Hardware Accelerated AI for Low Power at the Edge** (40 min)	Jordan Davies - Avnet Silica **Utilising Versal™ HBM** (40 min)	Francesco Contu - Avnet EMG Italy Srl (Silica) **Designing with high-speed interfaces, debugging techniques and design considerations** (40 min)	Christian Michel - Lattice Semiconductor GmbH **Golden System Reference Design (GSRD) - a rapid implementation concept for Soft-CPU based designs.** (90 min)
	Harry Commin - Enclustra GmbH **Fixed-Point Python Co-simulation** (40 min)		Patrice Brossard & Francisco Perez - Future Electronics S.A. **Artificial Intelligence in Low Power environment** (40 min)	Ernst Wehlage - PLC2 **Using RAM Resources efficiently for UltraScale+ based Devices** (40 min)	Oren Hollander - HandsOn Training **Hyperflex FPGA Architecture for Agilex 5 Devices** (40 min)	

FPGA Conference EUROPE

Program 2024

3 Days – 10 Thematic Focus Tracks – 100 Percent Knowhow

organized by ELEKTRONIK PRAXIS PLC2

Thursday, July 4

	Application	Board Design & Connectivity	Embedded	Tools & Methodologies	Architecture	Tutorials
9:00 am - 10:30 am	Patrick Urban - Cologne Chip AG **GateMate FPGA Bitstream Copy Protection using SRAMs** (40 min)	Shivani Saravanan - Intel Deutschland GmbH **altera Agilex® 5 FPGA IO Architecture and Variable-Pitch BGA Packaging** (40 min)	Ernst Wehlage - PLC2 & Jens Michaelsen - Avnet Silica **MicroBlaze V – the AMD way to do RISC-V** (90 min)	Alexander Flick - PLC2 **HLS and Vitis™ Libraries: A faithful companionship** (40 min)	Pascal Ravillion - Achronix Semiconductor Corporation **Addressing Flexibility in ASICs while using existing FPGA Implementations** (40 min)	Jim Lewis - SynthWorks Design Inc **Essential Steps to Simplify Testbenches Using OSVVM** (90 min)
	Helmut Demel - Lattice Semiconductor GmbH **Sensor Fusion applied to maximize accuracy for robots and lidar/radar applications** (40 min)	Marco Smutek - Arrow Central Europe GmbH **Comparing Power Consumption of FPGAs by altera Security** (40 min)		Alain Darte - AMD **Optimizing Your C++ Code to Implement High-Performance and Resource-Efficient Designs Using High-Level Synthesis Tools** (40 min)	Konstantin Dobrosolets - Intel Deutschland GmbH **altera Agilex® 5 FPGA Power and Performance Benefits** (40 min)	
10:30 - 11:00 am	**Coffee break**					
11:00 am - 12:30 am	Brian Colgan - Microchip Technology GmbH **Keeping cool: how to solve challenges in medical applications** (40 min)	Joachim Goertz - 3M **Rising Demand for High-Speed and High Bandwidth Interconnection** (40 min)	Salma Hamdoun - Arrow Central Europe GmbH **RISC-V Ecosystem/Mi-V** (40 min)	Ido Wermuth - Arrow Central Europe GmbH **Advantages of System Design with Low Power FPGAs** (40 min)	Tomasz Iwanski - Arrow Central Europe GmbH **altera® Hyperflex™: Fixing timings the fast way with Agilex™ FPGAs** (40 min)	Jim Lewis - SynthWorks Design Inc **Using OSVVM's AXI4 Verification Component** (90 min)
	Angelo Lo Cicero - Intel Deutschland GmbH **Robotics in altera FPGA** (40 min)	**To follow shortly (40 min)**	Klaus Kohl-Schöpe - Arrow Central Europe GmbH **RISC-V® on FPGA** (40 min)	Simon Heimbach - Universität Stuttgart **Automatic Evaluation and Partitioning of Algorithms for Heterogeneous Systems** (40 min)	Harald Werner - Efinix GmbH **Modern architectures of programmable devices** (40 min)	
12:30 - 1:30 pm	**Lunch break**					
1:30 pm - 3:00 pm	Oliver Bründler - Enclustra GmbH **All About AXI - Navigating Standards, Pitfalls and Implementation on Xilinx Devices** (40 min)	Karan Kantharia - AMD **Leveraging Kria SOMs for Faster Time to Market** (40 min)	Alexander Flick - PLC2 & Michal Pacula - Aldec **Creating a Versal AI Engine based Data Processing Design (PLC2) Part 1** (40 min)	Wolfgang Loewer - El Camino GmbH **Unlocking the Full Potential of Platform Designer from Intel** (40 min)	Harald Werner - Efinix GmbH **High Speed Interfaces** (40 min)	Adam Taylor - Adiuvo Engineering & Training Ltd **Perfecting PetaLinux – a hands on tutorial Part 1** (90 min)
	Prof. Dr. Bernhard Lang - Hochschule Osnabrück **High Performance Pipeline Processing with AXI-Streaming Components** (40 min)	Ernst Wehlage - PLC2 **The KRIA SOM Family and Design Flows** (40 min)	Michal Pacula - Aldec & Alexander Flick - PLC2 **Verifying Versal AI Engine based Designs for Optimal Performance (Aldec) Part 2** (40 min)	Shivani Saravanan - Intel Deutschland GmbH **Migrating to Quartus Pro** (40 min)	Maximilian Werner - Efinix GmbH **How to use and integrate MIPI CSI-2/DSI with Efinix FPGAs** (40 min)	
3:00 - 3:30 pm	**Coffee break**					
3:30 pm - 5:00 pm	Krzysztof Czyz - Embevity sp.zo. O **Optimizing FPGA Systems: A Case Study of employing SpinalHDL and VexRISCV core in Commercial Application.** (40 min)	Jordan Davies & Jens Michaelsen - Avnet Silica **Enhance your compute density :- Efficient hardware design, using SOM, SIP, IMC.** (40 min)	Fabian Heinrici - Efinix GmbH **Efinix RISC-V Solutions from soft to hard** (40 min)	Salma Hamdoun - Arrow Central Europe GmbH **FPGA Verification and Testing** (40 min)	Martin Kellermann - Microchip Technology GmbH **Intelligent and reliable industrial designs** (40 min)	Adam Taylor - Adiuvo Engineering & Training Ltd **Perfecting PetaLinux – a hands on tutorial Part 2** (90 min)
	Pablo Leyva Camacho - Citrobits GmbH **MIPI CSI2 on FPGAs, the unexpected challenges** (40 min)	Hüseyin Anaç - NCAB Group Germany GmbH **Ultra HDI PCBs – all you need to know about it** (40 min)	Dr. Riadh Ben Abdelhamid - Heidelberg University **Spanning an entire multi-die FPGA with 1,024 RISCV cores/16K Threads at 400MHz? yes you can!** (40 min)	Dr. Harald Simmler - Ing. Buero Harald Simmler **Efficient High Level Co-Simulation for HDL Designs** (40 min)	Bernhard Wandl - FH Oberösterreich Studienbetriebs GmbH - P2L2 GmbH. **High Performance Digital Radar on an AMD RFSoC FPGA** (40 min)	