

Training Calendar

2024

Training Formats

OL Online

Our PLC2 online training courses offer you the opportunity to acquire technical expertise in the desired and required depth. You can take part in the online training courses, which always take place on a half-day basis, from your home or office.

WE Webinar

The free 1-hour PLC2 webinars give participants a brief insight into a specific problem or topic. Our webinars shine with technical depth despite the limited time available. They are a good introduction to a certain topic.

SE Seminar

Our free 1-day PLC2 seminars give developers, team leaders, and company management staff a comprehensive insight into the numerous possibilities surrounding the use of programmable technologies.

Our competent instructors convey even difficult facts and contexts to you in an easily understandable way, while being present on-site. Individual questions and problems can be identified.

ES Easy Start

Our 2-day Easy Start training courses, which have been successful for years and are in great demand, were developed to make it easier for »newcomers« among FPGA and MPSoC users to get started in the FPGA/MPSoC field and to train and support them in the use of the technology. This training series is also suitable for project managers, team leaders and group leaders.

The focus of this training format is on practical application with modern FPGAs/MPSoCs and less on the theoretical basis. The participants will be professionally guided by our experienced PLC2 experts to implement their own FPGA/MPSoC projects in order to take the first steps towards independent development of complex FPGAs/MPSoCs. Deeper theoretical foundations are taught in other training courses.

WO Workshop

As the world's first and long-standing Authorized Training Provider (ATP) of Xilinx - today AMD, we always have access to brand-new technologies, methods, and development tools and work right at the forefront of the technological progress.

In our 2- and 3-day workshops, we share our knowledge with developers and train them in technical depth. During the training, the participant has the chance to consolidate and reinforce the knowledge imparted by our experts in practical exercises. The training portfolio ranges from workshops covering all HDL users to specific AMD technology training. The content focuses on methodologies for development and verification, the architecture of the latest building blocks, physical implementation, and the application of the highly complex development tools.

PW Power Workshop

In the 5-day Power Workshops, our experts provide developers with particularly hands-on training in technical depth. Here, care is taken to ensure that the knowledge imparted is consolidated in the form of practical exercises.

Under the guidance and supervision of our competent trainers, the participants work intensively with laptops/PCs and, if required, with evaluation boards. Complex tasks are implemented, and the functionality is proven with the help of the simulation and the evaluation board.

The Power Workshops are suitable for all those who want to dive deeply into a topic and attach a lot of importance to practical relevance.

LT Long Term Education

Are you new to the FPGA world and want to become an expert in a very short period of time? Then you found your solution. We at PLC2 turn engineers and technicians into FPGA experts. Our 3 months training program provides you with the entire know-how on the latest state-of-art AMD FPGAs and SoCs. Our comprehensive training material includes boards, software, labs, telephone support, and a personal mentor.

Architecture

OL Online

WO Workshop

PW Power Workshop

In today's competitive world of electronic engineering the difference is made at the system architectural level. Making the right choices at the start of your design makes the difference between mediocre versus excellent results. We at PLC2 can help you by providing training courses in the architecture area of the world's leading FPGAs from AMD. The workshops provide the foundation you need to get started with your FPGA development or to optimize your FPGA designs. Our classes are suited for both, FPGA newcomers and experienced developers.

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|---|--------|----------|-----------|----------|----------|----------|----------|---------------------|-----------|----------|-----------|----------|----------|----------|------------------|
| Compact FPGA 7 Series | WO | 2 | | | | | | all year on request | | | | | | | € 1,700 / 18 TCs |
| Compact FPGA 7 Series | OL | 2 | | | | | | all year on request | | | | | | | € 1,300 / 14 TCs |
| Professional FPGA | PW | 5 | | 19–23, S | | | 13–17, F | | 08–12, FR | | | 21–25, M | | | € 3,250 / 45 TCs |
| Professional FPGA | OL | 5 | | 19–23, O | | | | | | | | 21–25, O | | | € 2,800 / 35 TCs |
| Compact UltraScale/UltraScale+ | WO | 2 | | | 21–22, M | | | 24–25, FR | | | 26–27, F | | 21–22, S | | € 1,700 / 18 TCs |
| Compact UltraScale/UltraScale+ | OL | 2 | | | | 04–05, O | | | | | | 28–29, O | | | € 1,300 / 14 TCs |
| Zynq UltraScale+ MPSoC for the System Architect | WO | 2 | | | 11–12, S | | | 03–04, F | | | 12–13, FR | | | 19–20, M | € 1,700 / 18 TCs |
| Zynq UltraScale+ MPSoC for the System Architect | OL | 2 | | | | 17–18, O | | | | | | | 20–21, O | | € 1,300 / 14 TCs |
| Zynq 7000 SoC for the System Architect | WO | 2 | | | | | | all year on request | | | | | | | € 1,700 / 18 TCs |
| Zynq 7000 SoC for the System Architect | OL | 2 | | | | | | all year on request | | | | | | | € 1,300 / 14 TCs |
| Versal Adaptive SoC for the System Architect | WO | 2 | 15–16, FR | | | 15–16, F | | | | 01-02, S | | | 18–19, M | | € 1,700 / 18 TCs |
| Versal Adaptive SoC for the System Architect | OL | 2 | | | 21–22, O | | | | | | | | | 11–12, O | € 1,300 / 14 TCs |
| Essentials of Microprocessors | WO | 1 | | | | | | all year on request | | | | | | | € 800 / 9 TCs |
| Essentials of Microprocessors | OL | 1 | | | | | | all year on request | | | | | | | € 600 / 7 TCs |

Tools & Methodology ^{1/3}

The HDL-based development method simplifies the development cycle, but this requires the developer to have good knowledge of digital circuit design. It is not enough to know how to implement combinational and sequential circuits, it is very important to know how to implement your design in the FPGA architecture to maximize benefits in size, power, and performance.

The PLC2 training courses in the »Tools and Methodology« category help developers use and apply the development tools for these latest technologies.

OL Online
SE Seminar
ES Easy Start
WO Workshop
PW Power Workshop

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|--|--------|----------|-----------|-----------|----------|-----------|-----------|---------------------|-----------|----------|-----------|-----------|-----------|-----------|-----------------------------|
| Easy Start FPGA Vivado | ES | 2 | 22–23, FR | | 04–05, B | | 27–28, M | | | 08–09, S | | | 14–15, F | | € 2,050* / 18 TCs + € 350** |
| Easy Start FPGA Vivado | OL | 2 | | | | 15–16, O | | | 29–30, O | | | | | 04–05, O | € 1,300 / 14 TCs |
| FPGA Power Optimization | WO | 2 | | | | | | all year on request | | | | | | | € 1,700 / 18 TCs |
| FPGA Power Optimization | OL | 2 | | | | | | all year on request | | | | | | | € 1,300 / 14 TCs |
| Dynamic Function eXchange (DFX) | WO | 2 | 22–23, M | | | 11–12, F | | | 08–09, S | | | 01–02, FR | | | € 1,700 / 18 TCs |
| Dynamic Function eXchange (DFX) | OL | 2 | | | | 11–12, O | | | | | | 01–02, O | | | € 1,300 / 14 TCs |
| FPGA Circuit Design Technique | SE | 1 | | | 20, S | | | | | | 25, FR | | | | free of charge |
| Compact FPGA Circuit Design Technique | WO | 3 | 24–26, FR | | | | 22–24, F | | | 05–07, S | | 09–11, B | | | € 2,300 / 27 TCs |
| Compact FPGA Circuit Design Technique | OL | 3 | | | 04–06, O | | | 10–12, O | | | 16–18, O | | | 09–11, O | € 1,900 / 21 TCs |
| Professional FPGA Circuit Design Technique | PW | 5 | | 05–09, FR | | 08–12, FR | | | 15–19, FR | | | | 04–08, FR | | € 3,250 / 45 TCs |
| Professional FPGA Circuit Design Technique | OL | 5 | | | | 08–12, O | | | | | | | 04–08, O | | € 2,800 / 35 TCs |
| Git for EDA Tool Flows | WO | 3 | | | 04–06, S | | | 10–12, B | | | 09–11, M | | | 16–18, FR | € 2,300 / 27 TCs |
| Git for EDA Tool Flows | OL | 3 | | | | 10–12, O | | | | | | | 11–13, O | | € 1,900 / 21 TCs |
| Continuous Integration for EDA Tools | PW | 5 | | 05–09, S | | | 13–17, FR | | 08–12, F | | | 07–11, B | | | € 3,250 / 45 TCs |
| Continuous Integration for EDA Tools | OL | 5 | | | | | 13–17, O | | | | | 14–18, O | | | € 2,800 / 35 TCs |
| Compact Vivado Design Suite Tool Flow | WO | 2 | | 19–20, FR | | | | 03–04, F | | | 16–17, S | | 04–05, M | | € 1,700 / 18 TCs |
| Compact Vivado Design Suite Tool Flow | OL | 2 | | | 18–19, O | | | | 22–23, O | | | 07–08, O | | | € 1,300 / 14 TCs |

B Berlin F Frankfurt / Main FR Freiburg M Munich O Online S Stuttgart

* including board
** board

Tools & Methodology ^{2/3}

OL Online
 WO Workshop
 PW Power Workshop
 LT Long Term Education

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|--|--------|----------|---------|-----------|-------------------------------------|-------------------------------------|------------------------|-----------|----------|-----------|------------------------|-------------------------------------|-------------------------------------|----------|-------------------|
| Compact Timing Constraints and Analysis | WO | 3 | | 21–23, FR | | | | 05–07, F | | | 18–20, S | | 06–08, M | | € 2,300 / 27 TCs |
| Compact Timing Constraints and Analysis | OL | 3 | | | 20–22, O | | | | 24–26, O | | | 09–11, O | | | € 1,900 / 21 TCs |
| Professional Vivado | PW | 5 | | | 11–15, FR | | | | 22–26, F | | | 07–11, FR | | 09–13, F | € 3,250 / 45 TCs |
| Professional Vivado | OL | 5 | | | 11–15, O | | | | | | | 07–11, O | | | € 2,800 / 35 TCs |
| NEW Advanced Vivado | WO | 3 | | | | 15–17, FR | | | 10–12, S | | | 28–30, F | | | € 2,300 / 27 TCs |
| NEW Advanced Vivado | OL | 3 | | | | 15–17, O | | | | | | 28–30, O | | | € 1,900 / 21 TCs |
| Debugging Techniques Using the Vivado Logic Analyzer | WO | 2 | | 14–15, B | | | | 26–27, FR | | | 12–13, S | | | 02–03, F | € 1,700 / 18 TCs |
| Debugging Techniques Using the Vivado Logic Analyzer | OL | 2 | | 14–15, O | | | | | | | | | | 02–03, O | € 1,300 / 14 TCs |
| Compact Vitis for the Software Designer | WO | 3 | | 26–28, FR | | | 22–24, F | | | | 17–19, B | | | 16–18, M | € 2,300 / 27 TCs |
| Compact Vitis for the Software Designer | OL | 3 | | 26–28, O | | | | | | | | | | 16–18, O | € 1,900 / 21 TCs |
| Compact Vitis for Acceleration | WO | 3 | | 05–07, M | | | 27–29, B | | | 12–14, FR | | | 20–22, F | | € 2,300 / 27 TCs |
| Compact Vitis for Acceleration | OL | 3 | | 05–07, O | | | | | | | | | 20–22, O | | € 1,900 / 21 TCs |
| Compact Vitis AI | WO | 3 | | | 25–27, F | | | 10–12, FR | | | 23–25, S | | 04–06, B | | € 2,300 / 27 TCs |
| Compact Vitis AI | OL | 3 | | | 25–27, O | | | | | | | | 04–06, O | | € 1,900 / 21 TCs |
| Professional Vitis | PW | 5 | | | 18–22, F | | | 24–28, S | | 05–09, FR | | | 04–08, B | | € 3,250 o. 45 TCs |
| Professional Vitis | OL | 5 | | | 18–22, O | | | | | | | | 04–08, O | | € 2,800 / 35 TCs |
| FPGA Designer (Long Term) | LT | 16 | | | 07–08, FR 18–19, FR 26–27, FR | 02–03, FR 17–18, FR 29–30, FR | 06–07, FR 15–16, FR | | | | 10–11, FR 23–24, FR | 07–08, FR 16–17, FR 23–24, FR | 11–12, FR 18–19, FR 27–28, FR | | € 8,400* |

B Berlin F Frankfurt / Main FR Freiburg M Munich O Online S Stuttgart

Languages ^{1/2}

OL Online
SE Seminar
WO Workshop
PW Power Workshop

Familiarize yourself with the latest design methods to get the most out of your chosen technology. Learn the fundamentals and become an expert in HDL languages such as VHDL or System Verilog.

We offer a variety of workshops and training sessions to introduce you to System Verilog HDL and VHDL. You will learn the VHDL synthesis and simulation concept and understand how to use different synthesis or simulation constructs to design your FPGA.

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|---|--------|----------|----------|-----------|-----------|----------|-----------|-----------|-----------|----------|-----------|-----------|----------|-----------|------------------|
| Circuit Synthesis with VHDL | SE | 1 | | | | 09, F | | | | | | 15, S | | | free of charge |
| Compact VHDL for Synthesis | WO | 3 | 15–17, B | | 18–20, FR | | | 03–05, F | | | 02–04, S | | 04–06, M | | € 2,300 / 27 TCs |
| Compact VHDL for Synthesis | OL | 3 | | | | 15–17, O | | | | 12–14, O | | | 25–27, O | | € 1,900 / 21 TCs |
| Circuit Simulation with VHDL | SE | 1 | | | | | 22, FR | | | | | | 13, F | | free of charge |
| Compact VHDL for Simulation | WO | 2 | 18–19, B | | 21–22, FR | | | 06–07, F | | | 05–06, S | | 07–08, M | | € 1,700 / 18 TCs |
| Compact VHDL for Simulation | OL | 2 | | | | 18–19, O | | | | 15–16, O | | | 28–29, O | | € 1,300 / 14 TCs |
| Professional VHDL | PW | 5 | | 19–23, FR | | 22–26, M | | | 22–26, FR | | | 21–25, F | | 02–06, FR | € 3,250 / 45 TCs |
| Professional VHDL | OL | 5 | | | | 22–26, O | | | | | | 21–25, O | | | € 2,800 / 35 TCs |
| NEW Advanced VHDL | WO | 3 | | | 25–27, S | | | | 15–17, F | | | 28–30, FR | | 09–11, M | € 2,300 / 27 TCs |
| NEW Advanced VHDL | OL | 3 | | | | | 27–29, O | | | | | | | 16–18, O | € 1,900 / 21 TCs |
| Compact VHDL Testbenches and Verification with OSVVM | WO | 3 | | | 11–13, S | | 06–08, FR | | | 06–08, B | | 16–18, M | | | € 2,300 / 27 TCs |
| Compact VHDL Testbenches and Verification with OSVVM | OL | 3 | | 26–28, O | | | | 12–14, O | | | | | | 09–11, O | € 1,900 / 21 TCs |
| Professional VHDL Testbenches and Verification with OSVVM | PW | 5 | | 12–16, F | | | | 24–28, FR | | | 16–20, FR | | 18–22, S | | € 3,250 / 45 TCs |
| Professional VHDL Testbenches and Verification with OSVVM | OL | 5 | | 12–16, O | | | | | | | | | 18–22, O | | € 2,800 / 35 TCs |
| UVM Testbench Made Easy | WO | 2 | | 22–23, F | | 25–26, M | | | 25–26, B | | | 24–25, FR | | | € 1,700 / 18 TCs |
| UVM Testbench Made Easy | OL | 2 | | 22–23, O | | 25–26, O | | | 25–26, O | | | 24–25, O | | | € 1,300 / 14 TCs |

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Languages 2/2



Online



Workshop



Power Workshop

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|---|--------|----------|---------|----------|----------|----------|-----|-----------|-----------|--------|-----------|-----------|----------|----------|------------------|
| NEW Compact System Verilog for Synthesis | WO | 3 | | 05–07, S | | 08–10, F | | | 10–12, FR | | | 07–09, M | | | € 2,300 / 27 TCs |
| NEW Compact System Verilog for Synthesis | OL | 3 | | | | 03–05, O | | | | | | | 27–29, O | | € 1,900 / 21 TCs |
| SystemVerilog - Advanced Verification for FPGA Design | WO | 3 | | 19–21, F | | 22–24, M | | | 22–24, B | | | 21–23, FR | | | € 2,300 / 27 TCs |
| SystemVerilog - Advanced Verification for FPGA Design | OL | 3 | | 19–21, O | | 22–24, O | | | 22–24, O | | | 21–23, O | | | € 1,900 / 21 TCs |
| Compact Python for Embedded | WO | 3 | | | 04–06, S | | | 24–26, FR | | | 23–25, F | | 25–27, B | | € 2,300 / 27 TCs |
| Compact Python for Embedded | OL | 3 | | | 04–06, O | | | | | | | | 25–27, O | | € 1,900 / 21 TCs |
| Professional Python for Embedded | PW | 5 | | | 04–08, S | | | 24–28, FR | | | 23–27, F | | 25–29, B | | € 3,250 / 45 TCs |
| Professional Python for Embedded | OL | 5 | | | 04–08, O | | | | | | | | 25–29, O | | € 2,800 / 35 TCs |

Embedded 1/3

Are you a beginner in the embedded world or a very experienced embedded developer? We at PLC2 tailor our embedded classes to your level. Our workshops include everything you need to know on how to develop embedded solutions with AMD's wide range of SoCs. Understand the embedded design flow for the latest technologies from AMD including Versal adaptive SoC. There are software specific training topics on C/C++ as well as Linux and driver development under Linux.

- Online
- Easy Start
- Workshop
- Power Workshop

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|---|--|----------|---------|----------|-----------|-----------|-----------|---------------------|----------|----------|-----------|----------|-----------|-----------------------------|-----------------------------|
| Easy Start Embedded for Zynq UltraScale+ MPSoC Systems | ● ES | 2 | | | 11–12, S | | | | 15–16, F | | | 15–16, B | | 09–10, FR | € 1,700 / 18 TCs |
| NEW Easy Start Embedded Flow | ● ES | 2 | | | 07–08, FR | | | 24–25, F | | | 09–10, B | | 11–12, S | | € 2,050* / 18 TCs + € 350** |
| NEW Easy Start ML Application Design Flow | ● ES | 2 | | | | 11–12, FR | | | 17–18, F | | | 23–24, S | | 05–06, M | € 1,700 / 18 TCs |
| Compact Zynq UltraScale+ MPSoC for the Hardware Designer | ● WO | 3 | | 19–21, F | | | 06–08, FR | | | 20–22, B | | | 25–27, M | | € 2,300 / 27 TCs |
| Compact Zynq UltraScale+ MPSoC for the Hardware Designer | ● OL | 3 | | | | 03–05, O | | | 15–17, O | | | 14–16, O | | | € 1,900 / 21 TCs |
| Advanced Zynq UltraScale+ MPSoC for the Hardware Designer | ● WO | 3 | | | 26–28, M | | | 12–14, B | | | 25–27, F | | | 16–18, S | € 2,300 / 27 TCs |
| Advanced Zynq UltraScale+ MPSoC for the Hardware Designer | ● OL | 3 | | | 26–28, O | | | | | | | | | 16–18, O | € 1,900 / 21 TCs |
| Compact Zynq UltraScale+ MPSoC for the Software Designer | ● WO | 3 | | 26–28, S | | | 13–15, F | | | 06–08, B | | | 18–20, FR | | € 2,300 / 27 TCs |
| Compact Zynq UltraScale+ MPSoC for the Software Designer | ● OL | 3 | | | | 08–10, O | | | 29–31, O | | | 28–30, O | | | € 1,900 / 21 TCs |
| Professional Zynq UltraScale+ MPSoC | ● PW | 5 | | | 18–22, FR | | | 03–07, F | | | 16–20, FR | | | 02–06, F | € 3,250 / 45 TCs |
| Professional Zynq UltraScale+ MPSoC | ● OL | 5 | | | 18–22, O | | | | | | | | | 02–06, O | € 2,800 / 35 TCs |
| Easy Start Embedded for Zynq 7000 SoC Systems | ● ES | 2 | | | | | | all year on request | | | | | | € 2,050* / 18 TCs + € 350** | |
| Compact Zynq 7000 SoC for the Hardware Designer | ● WO | 3 | | | | | | all year on request | | | | | | € 2,300 / 27 TCs | |
| Compact Zynq 7000 SoC for the Hardware Designer | ● OL | 3 | | | | | | all year on request | | | | | | € 1,900 / 21 TCs | |
| Compact Zynq 7000 SoC for the Software Designer | ● WO | 3 | | | | | | all year on request | | | | | | € 2,300 / 27 TCs | |
| Compact Zynq 7000 SoC for the Software Designer | ● OL | 3 | | | | | | all year on request | | | | | | € 1,900 / 21 TCs | |

B Berlin F Frankfurt / Main FR Freiburg M Munich O Online S Stuttgart

* including board
** board

Embedded 2/3

OL Online
WO Workshop
PW Power Workshop

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|---|--------|----------|-----------|----------|----------|-----------|-----|---------------------|----------|-----------|-----------|----------|----------|----------|------------------|
| Professional Zynq 7000 SoC | PW | 5 | | | | | | all year on request | | | | | | | € 3,250 / 45 TCs |
| Professional Zynq 7000 SoC | OL | 5 | | | | | | all year on request | | | | | | | € 2,800 / 35 TCs |
| Expert Zynq 7000 SoC | PW | 5 | | | | | | all year on request | | | | | | | € 3,250 / 45 TCs |
| Expert Zynq 7000 SoC | OL | 5 | | | | | | all year on request | | | | | | | € 2,800 / 35 TCs |
| Compact Versal Adaptive SoC for the Hardware Designer | WO | 3 | 17–19, FR | | | 17–19, F | | | 10–12, M | | | 16–18, S | | | € 2,300 / 27 TCs |
| Compact Versal Adaptive SoC for the Hardware Designer | OL | 3 | | | | 17–19, O | | | | | | 16–18, O | | | € 1,900 / 21 TCs |
| Compact Versal Adaptive SoC for the Software Designer | WO | 3 | | 14–16, S | | | | 03–05, F | | 12–14, FR | | 28–30, B | | | € 2,300 / 27 TCs |
| Compact Versal Adaptive SoC for the Software Designer | OL | 3 | | 14–16, O | | | | | | | | 28–30, O | | | € 1,900 / 21 TCs |
| Professional Versal Adaptive SoC | PW | 5 | | | 04–08, M | | | 10–14, FR | | | 02–06, F | | 11–15, S | | € 3,250 / 45 TCs |
| Professional Versal Adaptive SoC | OL | 5 | | | 04–08, O | | | | | | | | 11–15, O | | € 2,800 / 35 TCs |
| Advanced Versal Adaptive SoC AI Engine | WO | 3 | | | 13–15, S | | | 05–07, F | | | 09–11, FR | | | 04–06, M | € 2,300 / 27 TCs |
| Advanced Versal Adaptive SoC AI Engine | OL | 3 | | | 13–15, O | | | | | | | | | 04–06, O | € 1,900 / 21 TCs |
| Expert Versal Adaptive SoC AI Engine | PW | 5 | 22–26, S | | | 22–26, FR | | | 22–26, M | | | 07–11, F | | | € 3,250 / 45 TCs |
| Expert Versal Adaptive SoC AI Engine | OL | 5 | | | | 22–26, O | | | | | | 07–11, O | | | € 2,800 / 35 TCs |
| NEW Compact MicroBlaze System Design | WO | 3 | | | | | | all year on request | | | | | | | € 2,300 / 27 TCs |
| NEW Compact MicroBlaze System Design | OL | 3 | | | | | | all year on request | | | | | | | € 1,900 / 21 TCs |

B Berlin F Frankfurt / Main FR Freiburg M Munich O Online S Stuttgart

Embedded 3/3

- Online
- Seminar
- Easy Start
- Workshop
- Long Term Education

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|--|--------|----------|---------|----------|----------|------------------------|-------------------------------------|-------------------------------------|----------|----------|-----------|-------------------------------------|-------------------------------------|-----------------------------|-----------------------------|
| Developing Multimedia Solutions with the VCU and GStreamer | WO | 2 | | 14–15, S | | 18–19, FR | | | 29–30, F | | | 17–18, B | | | € 1,700 / 18 TCs |
| Developing Multimedia Solutions with the VCU and GStreamer | OL | 2 | | | | 18–19, O | | | | | | 17–18, O | | | € 1,300 / 14 TCs |
| Compact Embedded Linux | WO | 3 | | | 25–27, F | | | 17–19, M | | | 02–04, S | | 05–07, B | | € 2,300 / 27 TCs |
| Compact Embedded Linux | OL | 3 | | | 25–27, O | | | | | | | | 05–07, O | | € 1,900 / 21 TCs |
| Embedded Linux Driver Development | WO | 3 | | 05–07, M | | | 27–29, S | | | 05–07, B | | 16–18, F | | | € 2,300 / 27 TCs |
| Embedded Linux Driver Development | OL | 3 | | 05–07, O | | | | | | | | 16–18, O | | | € 1,900 / 21 TCs |
| Easy Start Embedded PetaLinux | ES | 2 | | | | | | all year on request | | | | | | € 2,050* / 18 TCs + € 350** | |
| Embedded Design with PetaLinux Tools | WO | 2 | | | 11–12, S | | | 26–27, F | | | 11–12, B | | 28–29, M | | € 1,700 / 18 TCs |
| Embedded Design with PetaLinux Tools | OL | 2 | | | 11–12, O | | | | | | | | 28–29, O | | € 1,300 / 14 TCs |
| Easy Start Kria for Vision Development | ES | 2 | | 22–23, F | | | 27–28, S | | | | 23–24, FR | | 05–06, B | | € 2,050* / 18 TCs + € 350** |
| Kria for the Software Developer | SE | 1 | | | | | | all year on request | | | | | | free of charge | |
| Embedded Designer (Long Term) | LT | 16 | | | | 03–04, FR 15–16, FR | 02–03, FR 13–14, FR 22–23, FR | 03–04, FR 12–13, FR 26–27, FR | | | | 01–02, FR 14–15, FR 21–22, FR | 06–07, FR 18–19, FR 25–26, FR | 02–03, FR 11–12, FR | € 8,400* |

B Berlin F Frankfurt / Main FR Freiburg M Munich O Online S Stuttgart

* including board
** board

DSP

OL Online
WO Workshop
PW Power Workshop

With their inherent flexibility, AMD FPGAs and SoCs are ideal for high-performance or multi-channel digital signal processing (DSP) applications that can take advantage of hardware parallelism. AMD FPGAs and SoCs combine this processing bandwidth with comprehensive solutions, including easy-to-use design tools for hardware designers, software developers, and system architects. We at PLC2 will teach you how to get the maximum out of these FPGAs and SoCs using Vitis Model Composer in interaction with Matlab Simulink. Additionally, you will learn how to develop HDL-based DSP functions.

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|--|--------|----------|---------|----------|----------|----------|----------|---------------------|----------|-----------|-----------|----------|----------|----------|------------------|
| Compact Vitis HLS | WO | 3 | | 14–16, F | | | 06–08, M | | | 27–29, FR | | | 27–29, S | | € 2,300 / 27 TCs |
| Compact Vitis HLS | OL | 3 | | | 18–20, O | | | | 29–31, O | | | 21–23, O | | | € 1,900 / 21 TCs |
| Compact DSP Design for FPGAs Using Vitis Model Composer | WO | 3 | | 05–07, M | | 08–10, F | | | | | 02–04, FR | | | 16–18, B | € 2,300 / 27 TCs |
| Compact DSP Design for FPGAs Using Vitis Model Composer | OL | 3 | | | | 08–10, O | | | | | | | | 16–18, O | € 1,900 / 21 TCs |
| Compact DSP Design for Versal Using Vitis Model Composer | WO | 3 | | | | | | all year on request | | | | | | | € 2,300 / 27 TCs |
| Compact DSP Design for Versal Using Vitis Model Composer | OL | 3 | | | | | | all year on request | | | | | | | € 1,900 / 21 TCs |
| Professional DSP Design Using Vitis Model Composer | PW | 5 | | 05–09, M | | 08–12, F | | | | | 02–06, FR | | | 16–20, B | € 3,250 / 45 TCs |
| Professional DSP Design Using Vitis Model Composer | OL | 5 | | | | 08–12, O | | | | | | | | 16–20, O | € 2,800 / 35 TCs |

Connectivity ^{1/2}

OL Online

WO Workshop

How do you keep up with the edge network emerging applications that are redefining hardware requirements for electronic designers? Are you designing the next generation AI for IoT, embedded vision, hardware security, 5G communication, or industrial/automotive automation for your company? Then PLC2 can teach you how the state-of-art AMD products can be used in your application for processing and bridging needs including high bandwidth sensor and display interfaces, video processing and machine learning inferencing.

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|---|--------|----------|----------|----------|-----------|----------|-----------|---------------------|------|----------|-----------|----------|-----------|------------------|------------------|
| AXI Interface Technology | WO | 2 | | | 05–06, FR | | | 26–27, F | | | 09–10, B | | 28–29, M | | € 1,700 / 18 TCs |
| AXI Interface Technology | OL | 2 | | | | 22–23, O | | | | 01–02, O | | | | 09–10, O | € 1,300 / 14 TCs |
| Compact Zynq UltraScale+ RFSoc | WO | 3 | | 14–16, B | | | 13–15, FR | | | | 16–18, F | | | 09–11, M | € 2,300 / 27 TCs |
| Compact Zynq UltraScale+ RFSoc | OL | 3 | | | | | 13–15, O | | | | | | | 09–11, O | € 1,900 / 21 TCs |
| Compact UltraScale: High-Speed Memory Interfacing | WO | 3 | | | | | | all year on request | | | | | | € 2,300 / 27 TCs | |
| Compact UltraScale: High-Speed Memory Interfacing | OL | 3 | | | | | | all year on request | | | | | | € 1,900 / 21 TCs | |
| Compact UltraScale: Serial Transceivers | WO | 3 | | 26–28, M | | | 06–08, B | | | | 23–25, F | | | | € 2,300 / 27 TCs |
| Compact UltraScale: Serial Transceivers | OL | 3 | | | | | 06–08, O | | | | | | 18–20, O | | € 1,900 / 21 TCs |
| Designing with Ethernet MAC Controllers | WO | 2 | 24–25, M | | | | 27–28, S | | | | 11–12, B | | 21–22, FR | | € 1,700 / 18 TCs |
| Designing with Ethernet MAC Controllers | OL | 2 | | | | 24–25, O | | | | | | | 13–14, O | | € 1,300 / 14 TCs |
| Compact Versal Adaptive SoC: Connectivity | WO | 3 | | | | 03–05, B | | | | 12–14, S | | | 04–06, F | | € 2,300 / 27 TCs |
| Compact Versal Adaptive SoC: Connectivity | OL | 3 | | | 18–20, O | | | | | | | 07–09, O | | | € 1,900 / 21 TCs |
| Compact UltraScale: Integrated PCI Express System | WO | 3 | | 05–07, S | | | 22–24, FR | | | | 02–04, M | | | 02–04, B | € 2,300 / 27 TCs |
| Compact UltraScale: Integrated PCI Express System | OL | 3 | | | | 15–17, O | | | | | | | 11–13, O | | € 1,900 / 21 TCs |
| Compact Versal Adaptive SoC: PCI Express Systems | WO | 2 | | | 04–05, M | | | 03–04, B | | | | 14–15, S | | | € 1,700 / 18 TCs |
| Compact Versal Adaptive SoC: PCI Express Systems | OL | 2 | | | 21–22, O | | | | | | | | 21–22, O | | € 1,300 / 14 TCs |

B Berlin F Frankfurt / Main FR Freiburg M Munich O Online S Stuttgart

Connectivity 2/2

 Online

 Workshop

| Training | Format | Duration | January | February | March | April | May | June | July | August | September | October | November | December | Fee |
|--|---|----------|---------|----------|-------|-------|-----|---------------------|------|--------|-----------|---------|----------|----------|------------------|
| Compact UltraScale: Board Design and Signal Integrity |  | 3 | | | | | | all year on request | | | | | | | € 2,300 / 27 TCs |
| Compact UltraScale: Board Design and Signal Integrity |  | 3 | | | | | | all year on request | | | | | | | € 1,900 / 21 TCs |
| Compact Versal Adaptive SoC: Power and Board Design |  | 3 | | | | | | all year on request | | | | | | | € 2,300 / 27 TCs |
| Compact Versal Adaptive SoC: Power and Board Design |  | 3 | | | | | | all year on request | | | | | | | € 1,900 / 21 TCs |