PLC2

Training Calendar

2023

Training Formats

OL Online

Our PLC2 online training courses offer you the opportunity to acquire technical expertise in the desired and required depth. You can take part in the online training courses, which always take place on a half-day basis, from your home or office.

WE Webinar

The free 1-hour PLC2 webinars give participants a brief insight into a specific problem or topic. Our webinars shine with technical depth despite the limited time available. They are a good introduction to a certain topic.

SE Seminar

Our free 1-day PLC2 seminars give developers, team leaders, and company management staff a comprehensive insight into the numerous possibilities surrounding the use of programmable technologies.

Our competent instructors convey even difficult facts and contexts to you in an easily understandable way, while being present on site. Individual questions and problems can be identified.

ES Easy Start

Our 2-day Easy Start training courses, which have been successful for years and are in great demand, were developed to make it easier for »newcomers« among FPGA and MPSoC users to get started in the FPGA/MPSoC field and to train and support them in the use of the technology. This training series is also suitable for project managers, team leaders and group leaders.

The focus of this training format is on practical application with modern FPGAs/MPSoCs and less on the theoretical basis. The participants will be professionally guided by our experienced PLC2 experts to implement their own FPGA/MPSoC projects in order to take the first steps towards independent development of complex FPGAs/MPSoCs. Deeper theoretical foundations are taught in other training courses.

WO Workshop

As the world's first and long-standing Authorized Training Provider of AMD Xilinx (ATP), we always have access to brand-new technologies, methods, and development tools and work right at the forefront of the technological progress.

In our 2- and 3-day workshops, we share our knowledge with developers and train them in technical depth. During the training, the participant has the chance to consolidate and reinforce the knowledge imparted by our experts in practical exercises. The training portfolio ranges from workshops covering all HDL users to specific AMD Xilinx technology training. The content focuses on methodologies for development and verification, the architecture of the latest building blocks, physical implementation, and the application of the highly complex development tools.

PW Power Workshop

In the 5-day Power Workshops, our experts provide developers with particularly hands-on training in technical depth. Here, care is taken to ensure that the knowledge imparted is consolidated in the form of practical exercises.

Under the guidance and supervision of our competent trainers, the participants work intensively with laptops/PCs and, if required, with evaluation boards. Complex tasks are implemented, and the functionality is proven with the help of the simulation and the evaluation board.

The Power Workshops are suitable for all those who want to dive deeply into a topic and attach a lot of importance to practical relevance.

LT Long Term Education

Are you new to the FPGA world and want to become an expert in a very short period of time? Then you found your solution. We at PLC2 turn engineers and technicians into FPGA experts. Our 3 months training program provides you with the entire know-how on the latest state-of-art AMD Xilinx FPGAs and SoCs. Our comprehensive training material includes boards, software, labs, telephone support and a personal mentor.

Architecture

In today's competitive world of electronic engineering the difference is made at the system architectural level. Making the right choices at the start of your design makes the difference between mediocre versus excellent results. We at PLC2 can help you by providing training courses in the architecture area of the world's leading FPGAs from AMD Xilinx. The workshops provide the foundation you need to get started with your FPGA development or to optimize your FPGA designs. Our classes are suited for both, FPGA newcomers and experienced developers.

OL Online WO Workshop PW Power Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Compact FPGA 7 Series	WO	2						all year on request							€ 1,700 / 18 TCs
Compact FPGA 7 Series	OL	2						all year on request							€ 1,300 / 14 TCs
Designing with the Spartan-7 Family	WO	2			01—02, FR			01—02, F			19—20, B		02—03, S		€ 1,850 / 18 TCs + € 150*
Designing with the Spartan-7 Family	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Professional FPGA	PW	5		06—10, S			22—26, F		24—28, FR			23—27, M			€ 3,250 / 45 TCs
Professional FPGA	OL	5						the whole year tbd							€ 2,800 / 35 TCs
Compact UltraScale/UltraScale+	WO	2			20—21, M			05—06, FR			14—15, F		15—16, S		€ 1,700 / 18 TCs
Compact UltraScale/UltraScale+	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Zynq UltraScale+ MPSoC for the System Architect	WO	2			23—24, S			01—02, F			14—15, FR			11—12, M	€ 1,700 / 18 TCs
Zynq UltraScale+ MPSoC for the System Architect	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Zynq-7000 SoC for the System Architect	WO	2		16—17, F				26—27, B			18—19, FR		29—30, M		€ 1,700 / 18 TCs
Zynq-7000 SoC for the System Architect	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Versal ACAP for the System Architect	WO	2	16—17, FR			10—11, F				07-08, S			02—03, M		€ 1,700 / 18 TCs
Versal ACAP for the System Architect	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Essentials of Microprocessors	WO	1						all year on request							€ 800 / 9 TCs
Essentials of Microprocessors	OL	1						all year on request							€ 600 / 7 TCs

B Berlin F Frankfurt / Main FR Freiburg M Munich S Stuttgart * including board

Tools & Methodology 1/2

OL Online SE Seminar ES Easy Start WO Workshop PW Power Workshop

The HDL based development method simplifies the development cycle, but this requires the developer to have good knowledge of digital circuit design. It is not enough to know how to implement combinational and sequential circuits, it is very important to know how to implement your design in the FPGA architecture to maximize benefits in size, power, and performance.

The PLC2 training courses in the »Tools and Methodology« category help developers use and apply the development tools for these latest technologies.

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Easy Start FPGA Vivado	ES	2	16–17, FR		01–02, B		15–16, M			10–11, S			20–21, F		€ 1,900 / 18 TCs + € 350*
Easy Start FPGA Vivado	OL	2						the whole year tbd							€ 1,300 / 14 TCs
FPGA Power Optimization	WO	2						all year on request							€ 1,700 / 18 TCs
FPGA Power Optimization	OL	2						all year on request							€ 1,300 / 14 TCs
Dynamic Function eXchange (DFX)	WO	2	16–17, M			17–18, F			17–18, S			30–31, FR			€ 1,700 / 18 TCs
Dynamic Function eXchange (DFX)	OL	2						the whole year tbd							€ 1,300 / 14 TCs
FPGA Circuit Design Technique	SE	1			22, M						27, FR				free of charge
Compact FPGA Circuit Design Technique	WO	3	18–20, FR				10–12, F			07–09, S		04–06, B			€ 2,300 / 27 TCs
Compact FPGA Circuit Design Technique	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional FPGA Circuit Design Technique	PW	5		13–17, FR		17–21, FR			17–21, FR				06–10, FR		€ 3,250 / 45 TCs
Professional FPGA Circuit Design Technique	OL	5						all year on request							€ 2,800 / 35 TCs
Git for EDA Tool Flows	WO	3			01–03, S			05–07, B			04–06, M			18–20, FR	€ 2,300 / 27 TCs
Git for EDA Tool Flows	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Continuous Integration for EDA Tools	PW	5		13–17, S			08–12, FR		10–14, F			09–13, B			€ 3,250 / 45 TCs
Continuous Integration for EDA Tools	OL	5						all year on request							€ 2,800 / 35 TCs
Vivado Design Suite Tool Flow	WO	1		06, FR				12, S			18, F		27, B		€ 800 / 9 TCs
Vivado Design Suite Tool Flow	OL	1						the whole year tbd							€ 600 / 7 TCs

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Tools & Methodology 2/2

OL Online WO Workshop PW Power Workshop LT Long Term Education

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Vivado Design Suite Static Timing Analysis and XILINX Design Constraints	WO	3		07–09, FR				13–15, S			19–21, F		28–30, B		€ 2,300 / 27 TCs
Vivado Design Suite Static Timing Analysis and XILINX Design Constraints	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional Vivado	PW	5			20–24, FR				10–14, F			09–13, FR		04–08, F	€ 3,250 / 45 TCs
Professional Vivado	OL	5						all year on request							€ 2,800 / 35 TCs
Debugging Techniques Using the Vivado Logic Analyzer	WO	2		27–28, B				01–02, FR			28–29, S			04–05, F	€ 1,700 / 18 TCs
Debugging Techniques Using the Vivado Logic Analyzer	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Designing with the XILINX Analog Mixed Signal Solution	WO	2						all year on request							€ 1,700 / 18 TCs
Designing with the XILINX Analog Mixed Signal Solution	OL	2						all year on request							€ 1,300 / 14 TCs
Compact Vitis for the Software Designer	WO	3		22–24, FR			03–05, F				05–07, B			18–20, M	€ 2,300 / 27 TCs
Compact Vitis for the Software Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Vitis for Acceleration	WO	3		01–03, M			23–25, B			01–03, FR			22–24, F		€ 2,300 / 27 TCs
Compact Vitis for Acceleration	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Vitis AI	WO	3			01–03, F			05–07, FR			18–20, S		20–22, B		€ 2,300 / 27 TCs
Compact Vitis AI	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional Vitis	PW	5			27–31, F			12–16, S		07–11, FR			13–17, B		€ 3,250 o. 45 TCs
Professional Vitis	OL	5						all year on request							€ 2,800 / 35 TCs
FPGA Designer	LT	16			06–07, FR 15–16, FR 28–29, FR	03–04, FR 18–19, FR 26–27, FR	08–09, FR 22–23, FR				12–13, FR 25–26, FR	09–10, FR 18–19, FR 25–26, FR	02–03, FR 13–14, FR 22–23, FR		€ 8,400

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Languages 1/2

Familiarize yourself with the latest design methods to get the most out of your chosen technology. Learn the fundamentals and become an expert in HDL languages such as VHDL or System Verilog.

We offer a variety of workshops and training sessions to introduce you to System Verilog HDL and VHDL. You will learn the VHDL synthesis and simulation concept and understand how to use different synthesis or simulation constructs to design your FPGA.

OL Online SE Seminar WO Workshop PW Power Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Circuit Synthesis with VHDL	SE	1				04, F						17, S			free of charge
Compact VHDL for Synthesis	WO	3	16–18, B		27–29, FR			19–21, F			18–20, S		06–08, M		€ 2,300 / 27 TCs
Compact VHDL for Synthesis	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Circuit Simulation with VHDL	SE	1					16, FR						14, F		free of charge
Compact VHDL for Simulation	WO	2	19–20, B		30–31, FR			22–23, F			21–22, S		09–10, M		€ 1,700 / 18 TCs
Compact VHDL for Simulation	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Professional VHDL	PW	5		06–10, FR		24–28, M			24–28, FR			23–27, FR		11–15, FR	€ 3,250 / 45 TCs
Professional VHDL	OL	5						all year on request							€ 2,800 / 35 TCs
Compact VHDL Testbenches and Verification with OSVVM	WO	3			20–22, S		22–24, FR			08–10, B			27–29, M		€ 2,300 / 27 TCs
Compact VHDL Testbenches and Verification with OSVVM	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional VHDL Testbenches and Verification with OSVVM	PW	5		20–24, F				12–16, FR			11–15, FR		20–24, S		€ 3,250 / 45 TCs
Professional VHDL Testbenches and Verification with OSVVM	OL	5						all year on request							€ 2,800 / 35 TCs
Compact Verilog	WO	3						all year on request							€ 1,900 / 21 TCs
Compact Verilog	OL	3						all year on request							€ 2,300 / 27 TCs
UVM Made Easy for FPGA Designers	WO	2		09–10, F		27–28, M			27–28, B			19–20, FR			€ 1,700 / 18 TCs
UVM Made Easy for FPGA Designers	OL	2		09–10, O		27–28, O			27–28, O			19–20, O			€ 1,300 / 14 TCs

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Languages 2/2

OL Online WO Workshop PW Power Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
SystemVerilog - Advanced Verification for FPGA Design	WO	3		06–08, F		24–26, M			24–26, B			16–18, FR			€ 2,300 / 27 TCs
SystemVerilog - Advanced Verification for FPGA Design	OL	3		06–08, O		24–26, O			24–26, O			16–18, O			€ 1,900 / 21 TCs
Compact Python for Embedded	WO	3			20–22, S			26–28, FR			25–27, F		20–22, B		€ 2,300 / 27 TCs
Compact Python for Embedded	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional Python for Embedded	PW	5			20–24, S			26–30, FR			25–29, F		20–24, B		€ 3,250 / 45 TCs
Professional Python for Embedded	OL	5						all year on request							€ 2,800 / 35 TCs

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Embedded 1/3

Are you a beginner in the embedded world or a very experienced embedded developer? We at PLC2 tailor our embedded classes to your level. Our workshops include everything you need to know on how to develop embedded solutions with AMD Xilinx wide range of SoCs. Understand the embedded design flow for the latest technologies from AMD Xilinx including Versal ACAP. There are software specific training topics on C/C++ as well as Linux and driver development under Linux.

OL Online ES Easy Start WO Workshop PW Power Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Easy Start Embedded for Zynq UltraScale+ MPSoC Systems	ES	2			16—17, S				12—13, F			30—31, B		04—05, FR	€ 1,700 / 18 TCs
Compact Zynq UltraScale+ MPSoC for the Hardware Designer	WO	3		13—15, F			15—17, FR			22—24, B			13—15, M		€ 2,300 / 27 TCs
Compact Zynq UltraScale+ MPSoC for the Hardware Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Advanced Zynq UltraScale+ MPSoC for the Hardware Designer	WO	3			27—29, M			21—23, B			11—13, F			06—08, S	€ 2,300 / 27 TCs
Advanced Zynq UltraScale+ MPSoC for the Hardware Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Zynq UltraScale+ MPSoC for the Software Designer	WO	3		22—24, S			10—12, F			01—03, B			06—08, FR		€ 2,300 / 27 TCs
Compact Zynq UltraScale+ MPSoC for the Software Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional Zynq UltraScale + MPSoC	PW	5			06—10, FR			12—16, F			25—29, FR			11—15, F	€ 3,250 / 45 TCs
Professional Zynq UltraScale + MPSoC	OL	5						all year on request							€ 2,800 / 35 TCs
Easy Start Embedded for Zynq-7000 SoC Systems	ES	2		27—28, FR			08—09, F		10—11, M			04—05, S			€ 1,900 / 18 TCs + € 350*
Compact Zynq-7000 SoC for the Hardware Designer	WO	3			13—15, S			05—07, FR			25—27, F			18—20, M	€ 2,300 / 27 TCs
Compact Zynq-7000 SoC for the Hardware Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Zynq-7000 SoC for the Software Designer	WO	3			20—22, M			28—30, B			11—13, FR		22—24, F		€ 2,300 / 27 TCs
Compact Zynq-7000 SoC for the Software Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs

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Embedded 2/3

OL Online WO Workshop PW Power Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Professional Zynq-7000 SoC	PW	5	23–27, FR			17–21, F			24–28, FR			16–20, F			€ 3,250 / 45 TCs
Professional Zynq-7000 SoC	OL	5						all year on request							€ 2,800 / 35 TCs
Expert Zynq-7000 SoC	PW	5						all year on request							€ 3,250 / 45 TCs
Expert Zynq-7000 SoC	OL	5						all year on request							€ 2,800 / 35 TCs
Compact Versal ACAP for the Hardware Designer	WO	3	18–20, FR			19–21, F			17–19, M			18–20, S			€ 2,300 / 27 TCs
Compact Versal ACAP for the Hardware Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Versal ACAP for the Software Designer	WO	3		01–03, S			03–05, F			09–11, FR		25–27, B			€ 2,300 / 27 TCs
Compact Versal ACAP for the Software Designer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Professional Versal ACAP	PW	5			06–10, M			19–23, S			25–29, F		13–17, FR		€ 3,250 / 45 TCs
Professional Versal ACAP	OL	5						all year on request							€ 2,800 / 35 TCs
Advanced Versal ACAP AI Engine	WO	3			01–03, S			26–28, F			20–22, FR			06–08, M	€ 2,300 / 27 TCs
Advanced Versal ACAP AI Engine	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Expert Versal ACAP AI Engine	PW	5	23–27, S			24–28, FR			17–21, M			09–13, F			€ 3,250 / 45 TCs
Expert Versal ACAP AI Engine	OL	5						all year on request							€ 2,800 / 35 TCs
Professional MicroBlaze System Design	PW	5						all year on request							€ 3,250 / 45 TCs
Professional MicroBlaze System Design	OL	5						all year on request							€ 2,800 / 35 TCs

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Embedded 3/3

OL Online SE Seminar ES Easy Start WO Workshop LT Long Term Education

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Developing Multimedia Solutions with the VCU and GStreamer	WO	2		27–28, S		03–04, FR			19–20, F			30–31, B			€ 1,700 / 18 TCs
Developing Multimedia Solutions with the VCU and GStreamer	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Compact Embedded Linux	WO	3			27–29, F			19–21, M			04–06, S		06–08, B		€ 2,300 / 27 TCs
Compact Embedded Linux	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Embedded Linux Development with Yocto Project	WO	2			30–31, F			22–23, M			07–08, S		09–10, B		€ 1,700 / 18 TCs
Embedded Linux Development with Yocto Project	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Embedded Linux Driver Development	WO	3		13–15, M			22–24, S			14–16, B		09–11, F			€ 2,300 / 27 TCs
Embedded Linux Driver Development	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Easy Start Embedded PetaLinux	ES	2						all year on request							€ 1,900 /18 TCs + € 350*
Embedded Design with PetaLinux Tools	WO	2			30–31, S			26–27, F			19–20, B		16–17, M		€ 1,700 / 18 TCs
Embedded Design with PetaLinux Tools	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Easy Start KRIA for Vision Development	ES	2		16–17, F			16–17, B				14–15, FR		20–21, S		€ 1,900 / 18 TCs + € 350*
Kria for Software Developers	SE	1				25, B	04, M 11, D								free of charge
Embedded Designer	LT	16				05–06, FR 20–21, FR	03–04, FR 10–11, FR 24–25, FR	05–06, FR 19–20, FR 28–29, FR				04–05, FR 16–17, FR 23–24, FR	08–09, FR 20–21, FR 27–28, FR	04–05, FR 13–14, FR	€ 8,400

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DSP

OL Online WO Workshop PW Power Workshop

With their inherent flexibility, AMD Xilinx FPGAs and SoCs are ideal for high-performance or multi-channel digital signal processing (DSP) applications that can take advantage of hardware parallelism. AMD Xilinx FPGAs and SoCs combine this processing bandwidth with comprehensive solutions, including easy-to-use design tools for hardware designers, software developers, and system architects. We at PLC2 will teach you how to get the maximum out of these FPGAs and SoCs using Vitis Model Composer in interaction with Matlab Simulink. Additionally, you will learn how to develop HDL based DSP functions.

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Vitis HLS	WO	3		13–15, F			15–17, M			16–18, FR			22–24, S		€ 2,300 / 27 TCs
Vitis HLS	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact DSP Design for FPGAs using Vitis Model Composer	WO	3		06–08, M		24–26, F					04–06, FR			18–20, B	€ 2,300 / 27 TCs
Compact DSP Design for FPGAs using Vitis Model Composer	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact DSP Design for Versal using Vitis Model Composer	WO	3						all year on request							€ 2,300 / 27 TCs
Compact DSP Design for Versal using Vitis Model Composer	OL	3						all year on request							€ 1,900 / 21 TCs
Professional DSP Design using Vitis Model Composer	PW	5		06–10, M		24–28, F					04–08, FR			18–22, B	€ 3,250 / 45 TCs
Professional DSP Design using Vitis Model Composer	OL	5						all year on request							€ 2,800 / 35 TCs

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Connectivity 1/2

How do you keep up with the edge network emerging applications that are redefining hardware requirements for electronic designers? Are you designing the next generation AI for IoT, embedded vision, hardware security, 5G communication, or industrial/automotive automation for your company? Then PLC2 can teach you how the state-of-art AMD Xilinx products can be used in your application for processing and bridging needs including high bandwidth sensor and display interfaces, video processing and machine learning inferencing.

OL Online WO Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
AXI Interface Technology	WO	2			13–14, FR			26–27, F			21–22, B		16–17, M		€ 1,700 / 18 TCs
AXI Interface Technology	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Compact Zynq UltraScale+ RFSoC	WO	3		06–08, B			22–24, FR				18–20, F			04–06, M	€ 2,300 / 27 TCs
Compact Zynq UltraScale+ RFSoC	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact UltraScale: High-Speed Memory Interfacing	WO	3						all year on request							€ 2,300 / 27 TCs
Compact UltraScale: High-Speed Memory Interfacing	OL	3						all year on request							€ 1,900 / 21 TCs
Compact UltraScale: Serial Transceivers	WO	3		13–15, M			03–05, B				04–06, F				€ 2,300 / 27 TCs
Compact UltraScale: Serial Transceivers	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Designing with Ethernet MAC Controllers	WO	2	18–19, M				22–23, S				21–22, B		09–10, FR		€ 1,700 / 18 TCs
Designing with Ethernet MAC Controllers	OL	2						the whole year tbd							€ 1,300 / 14 TCs
Compact Versal ACAP: Connectivity	WO	3				03–05, B				28–30, S			06–08, F		€ 2,300 / 27 TCs
Compact Versal ACAP: Connectivity	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact UltraScale: Integrated PCI Express System	WO	3		01–03, S			08–10, FR				11–13, M			11–13, B	€ 2,300 / 27 TCs
Compact UltraScale: Integrated PCI Express System	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Versal ACAP: PCI Express Systems	WO	2			27–29, M			12–14, B				16–18, S			€ 1,700 / 18 TCs
Compact Versal ACAP: PCI Express Systems	OL	2						the whole year tbd							€ 1,300 / 14 TCs

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Connectivity 2/2

OL Online WO Workshop

Training	Format	Duration	January	February	March	April	May	June	July	August	September	October	November	December	Fee
Compact UltraScale: Board Design and Signal Integrity	WO	3						the whole year tbd							€ 2,300 / 27 TCs
Compact UltraScale: Board Design and Signal Integrity	OL	3						the whole year tbd							€ 1,900 / 21 TCs
Compact Versal ACAP: Power and Board Design	WO	3						the whole year tbd							€ 2,300 / 27 TCs
Compact Versal ACAP: Power and Board Design	OL	3						the whole year tbd							€ 1,900 / 21 TCs

B Berlin F Frankfurt / Main FR Freiburg M Munich S Stuttgart