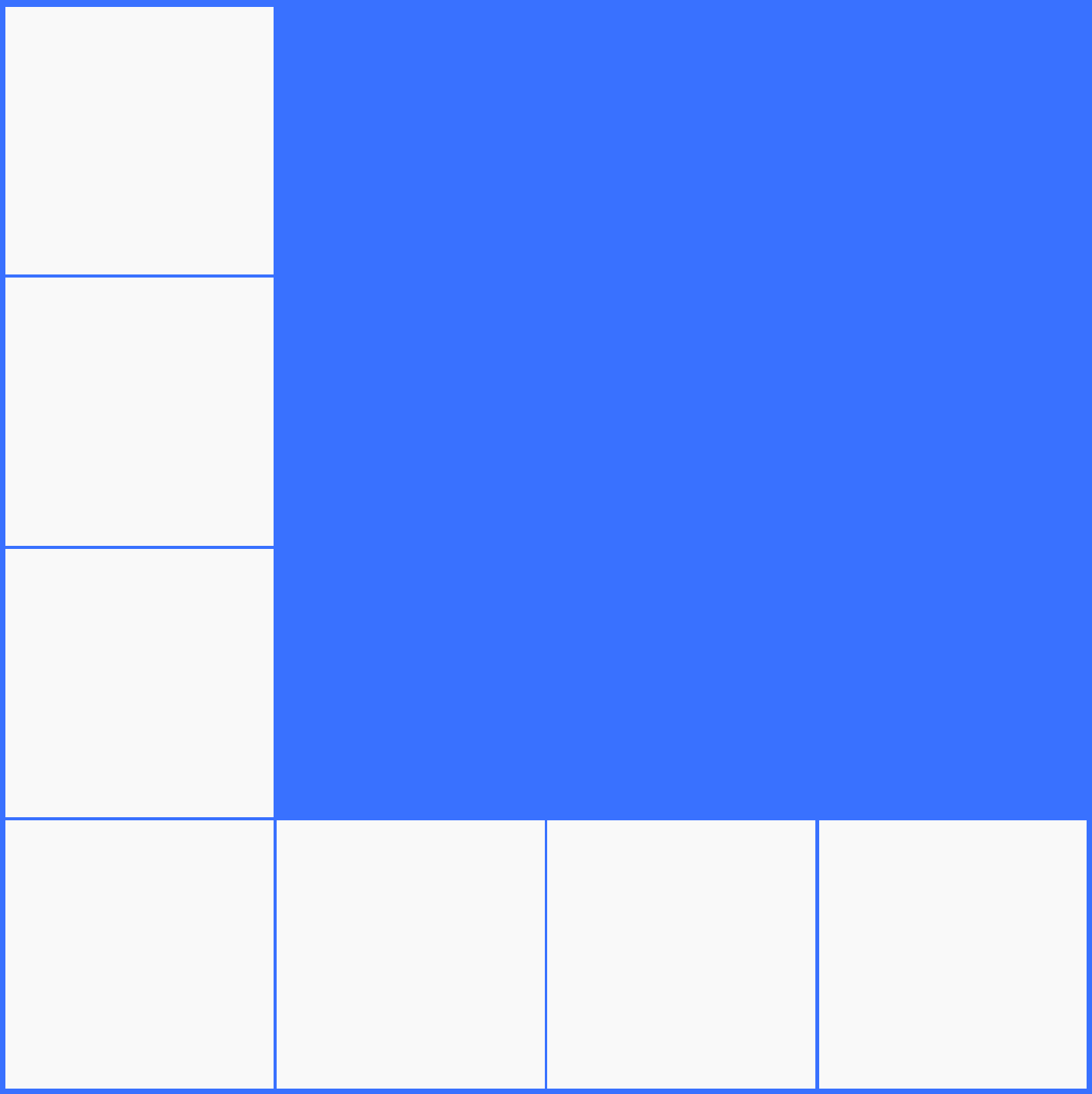
L5
(De-)Compression IP

PLC2

High Throughput, Low Latency, Lightweight and Lossless Performance at Ultra-Low Power.

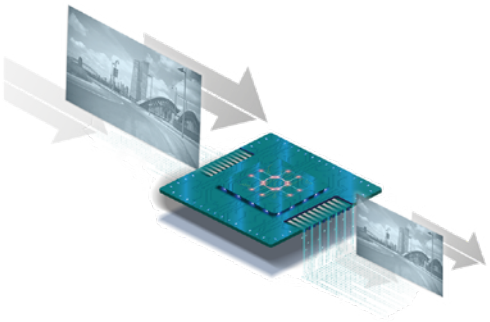


Maximum Compression with a Minimal Footprint in Size and Power

The PLC2 lossless, low latency, low power, and lightweight L5 (De-)Compression IP is a compression IP for nowadays data acquisition and processing systems. Special features make it possible to integrate the (de-)compression IP in existing AMD Xilinx FPGA-based designs and thus save time and costs.

The L5 (De-)Compression IP can achieve state-of-the-art subframe latency and low power consumption, without the need to invest in new and powerful hardware. Additional benefits include lightweight implementation in terms of resource consumption and lossless decompression for a wide range of applications at the edge and in the cloud. With this unique combination of assets, this core can be easily integrated into various scenarios, such as camera-based applications in the automotive industry, railway applications, robots, and/or drones. L5 reduces system storage costs, without adding significant latency to the overall system, and can reduce bandwidth needs at low power consumption.

The L5 accurately reflects our mission to deliver high-quality, high-performance solutions for tomorrow's technologies. This core is a unique solution to extend our capabilities within the field of data acquisition and processing and is in line with our vision and mission towards the future of an electrified vision zero.



Benefits of the L5

01 Reduced storage costs

02 Extended fleet time on the road

03 Flexible integration into existing solutions - from edge to cloud, from FPGA-accelerated to software processed

04 Integrated in the whole product chain for acquisition and replay

05 Lower bandwidth expenses

06 Support for multiple image types and architectures

Savings on average 30 – 70 %	Power estimation 0.05 W	Frame latency < 1 frame	Bandwidth up to 10 Gbit/s

Details

Lossless

The L5 fulfills all requirements for not losing a single bit within an image to ensure correct behavior of the attached system. We see a camera as a sensor and the image as a measure. All changes to the measure are also changing the reaction, which is then based on a wrong assumption. L5 Compression is truly lossless to prevent issues in that manner.

Lightweight

The L5 Compression IP is designed to have standard interfaces like AXI4-Stream and to be compatible with the AXI4-Stream Video Protocol of AMD. Additionally, the resource usage fits even into the smallest FPGAs and is easily adaptable for different architectures. it also does not require external resources like DDR memory.

Low power

Using the L5 Compression IP with its small resource usage makes it optimal for all applications needing lossless image compression without spending an additional power-consuming chip or requiring power-expensive external memory accesses.

Low latency

The L5 core is designed to have a latency of below one frame time for the whole transmission chain (encoding and decoding together). We can achieve that in addition without the need for external memory.

Specifications

General

Storage savings	~ 30 - 70 %
Power estimation*	< 0.05 W
Frame latency	< 1 frame

*Resolution: 2.4 MP, 16 bpp/processing at 100 MHz with 2 pixel per beat/on own data-set

Features

Formats	Bayer Pattern (RCCG, RGGB, RCCC, etc.) Gray, YUV422 Stereo-disparity RYYCy
Bit depths	Up to 16 bit
Resolutions	Configurable

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