FPGA Conference Europe Program 2023

	Tuesday - July 4				
	Application	**Language/Debug/Verification**	**Architecture**	**Embedded**	**Tutorials**
09:00 am - 10:30 am	Klaus Kohl-Schöppe - Arrow Central Europe GmbH **RISC-V® on Intel® FPGA** (English, 45 Min)	Espen Tallaksen - EmLogic AS **Good FPGA quality through efficient Verification – for beginners** (English, 45 Min)	Oren Hollander - HandsOn Training **Side Channel & Fault Injection Attacks on Modern FPGAs** (English, 45 Min)	Ernst Wehlage - PLC2 GmbH **Linux Build Methodologies: PetaLinux vs. Yocto Flow** (English, 45 Min)	Nikolai Krassin - PLC2 GmbH **Easy Start FPGA Vivado Part 1: Introduction to the FPGA Development Process** (English, 90 Min)
	Daire McNamara & Martin Kellermann - Emdalo Technologies, Microchip Technology **RISC-V with asymmetric multiprocessing for robotic applications** (English, 45 Min)	Espen Tallaksen - EmLogic AS **Get the right FPGA quality through efficient Specification Coverage (aka Requirement Coverage)** (English, 45 Min)	Thomasz Iwanski - Arrow Central Europe GmbH **Designing with Intel Hyperflex** (English, 45 Min)	Dr. Oliver Kühlert - SYSGO GmbH **Integrated RTOS and hypervisor ecosystem for MPU and MMU-based processors** (English, 45 Min)	
10:30 - 11:15 am	**Coffee break**				
11:15 am - 12:45 pm	Dr. Karsten Trott - AMD Xilinx **Random Number Generators for FPGAs and SoCs** (Englisch, 45 Min)	Hans-Jürgen Schwender - TRIAS Mikroelektronik GmbH **Using property descriptions to formally verify FPGA design code** (Englisch, 45 Min)	Martin Kellermann - Microchip Technology GmbH **Creating and securing your future with the RISC-V open instruction set architecture (ISA)** (Englisch, 45 Min)	Ernst Wehlage - PLC2 GmbH **Vitis Embedded Flow and managing the Software Projects** (Englisch, 90 Min)	Nikolai Krassin - PLC2 GmbH **Easy Start FPGA Vivado Part 2: FPGS Design Techniques** (Englisch, 90 Min)
	Andreas Schuler + Ulrich Langenbach - Missing Link Electronics GmbH **High Performance Smart NICs with FPGAs - Corundum with NPAP** (Englisch, 45 Min)	Patrick Lehmann - PLC2 GmbH **Synthesizing a Vivado Project on GitLab-CI and Deploying to an FPGA Board** (Englisch, 45 Min)	Jens Michaelsen - Avnet Silica **RISC-V, from toy to tool : The new mainstream CPU Instruction Set for FPGA.** (Englisch, 45 Min)		
12:45 - 1:45 pm	**Lunch break**				
1:45 - 2:15 pm	**KEYNOTE: Lattice Semiconductor Corporation - David Thomas**				
2:15 pm - 3:45 pm	Satheesh Chellappan & Masashi Tayama - Lattice Semiconductor **Secure method of enabling multiple design in FPGA** (English, 45 Min)	Jim Lewis - SynthWorks Design Inc **The post COVID update of OSVVM, VHDL's #1 Verification Methodology** (English, 45 Min)	Ron Renwick - Achronix Semiconductor Corporation **Utilizing Achronix FPGAs to Accelerate High Performance Networking Applications at 400GbE** (English, 45 Min)	Martin Kellermann - Microchip Technology GmbH **Optional peripherals: opening the hardware world for software engineers** (English, 45 Min)	Nikolai Krassin - PLC2 GmbH **Easy Start FPGA Vivado Part 3: VHDL Synthesis and Simulation** (English, 90 Min)
	Patrick Lehmann - PLC2 GmbH **Constraining Multiple Clock Domains** (English, 45 Min)	Jim Lewis - SynthWorks Design Inc **OSVVM's Test Reports and Simulator Independent Scripting** (English, 45 Min)	Scott Senst - Achronix Semiconductor Corporation **IP replication and partial reconfiguration using an FPGA with 2D NoC** (English, 45 Min)	Georg Hanak - Avnet EMG GmbH **AMD-Xilinx: Abstract Shell** (English, 45 Min)	
3:45 - 4:30 pm	**Coffee break**				
4:30 pm - 6:00 pm	Dr. Jörg Pospiech - AVT GmbH Ilmenau **Fast FPGS - Development with Ultra-SOM** (English, 45 Min)	Stefan Unrein - plc2 Design GmbH **How to properly simulate AXI4(Stream) with OSVVM -** (English, 90 Min)	Oliver Bründler - Enclustra GmbH **Key Considerations in FPGA-based Vision Systems** (English, 45 Min)	Georg Hanak - Avnet EMG GmbH **AMD-Xilinx: Dynamic Function Exchange with Device Tree Overlay** (English, 45 Min)	Nikolai Krassin - PLC2 GmbH **Easy Start FPGA Vivado Part 4: VHDL Finite State Machines** (English, 90 Min)
	Michael Freitag - YAGEO Corporation **New approach with FLEX to Reference Design** (English, 45 Min)		Prof. Dr. Bernhard Lang - Hochschule Osnabrück **GDBServer in Hardware for VexRiscv Processing Systems** (English, 45 Min)	Jörg Siemers - Avnet EMG GmbH **Performance Monitoring in Xilinx MPSoC devices** (English, 45 Min)	
6:00 - 6:30 pm	**Lucky Draw**				
from 7:00 pm	**Evening event with BBQ in the hotel restaurant of the NH München Ost Conference Center**				

	Wednesday - July 5				
	Application	**System on Module**	**Tools & Methodologies**	**Architecture**	**Tutorial**
09:00 am - 10:30 am	Matthias Schaffland - Sensor to Image GmbH **Next Generation of High-Speed Interfaces for Vision Applications** (English, 45 min)	Alexander Flick - PLC2 GmbH **Kria KR26 on the Vision and Robotics Starter Kits** (English, 90 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Vitis AI – design flow and the new features** (English, 45 min)	Ernst Wehlage - PLC2 GmbH **AMD Xilinx Zynq SoC/MPSoC vs. Versal Adaptive SoC (ASoC)** (English, 90 min)	Jim Lewis SynthWorks Design Inc **Faster than "Lite" Verification Component Development with OSVVM** (English, 90 min)
	Thomas Zerrer - Smartlogic GmbH **DMA data transmission with PCI-Express** (English, 45 min)		Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Demystify a Vitis Embedded Acceleration Platform** (English, 45 min)		
10:30 - 11:15 am	**Coffee break**				
11:15 am - 12:45 pm	Tom Richter - The MathWorks GmbH **5G NR Design - From Waveform Generation to Hardware Implementation and Verification** (English, 45 min)	Marco Höfle - Avnet EMG GmbH Silica **Workshop on an AMD Kria Platform demonstrating Software Acceleration in FPGA Logic: Deploying C/C++ Code with AMD Vitis** (English, 90 min)	Gerhard Nedok - Arrow Central Europe GmbH **Quartus Pro for Standard Users** (English, 45 min)	Ernst Wehlage - PLC2 GmbH **MicroBlaze - A most flexible processor for FPGAs and MPSoCs** (English, 45 min)	Jim Lewis SynthWorks Design Inc **OSVVM Testbench** (English, 90 min)
	Mustafa Celik - Arrow Central Europe GmbH **Time-Sensitive Networking with Intel Agilex 5** (English, 45 min)		Dr. Harald Simmler - hema elektronik GmbH **Self organizing administration tool to control FPGA designs** (English, 45 min)	Patrice Brossard + Baris Konuk - Future Electronics **Power efficiency in the Fpga world** (English, 45 min)	
12:45 - 1:30 pm	**Lunch break**				
1:30 - 2:15 pm	**Couch talk**				
2:15 pm - 3:45 pm	Karl Wachswender - Lattice Semiconductor Corporation **FPGA as bridging device in IIoT** (English, 45 min)	Sören Heß - plc2 Design GmbH **Introduction to Robotics Accerleration for FPGA Logic Design Engineers** (English, 90 min)	Wolfgang Loewer - El Camino GmbH **Fundamentals of Timing Analysis and Why No FPGA Design Can Do Without It** (English, 90 min)	Alexander Flick - PLC2 GmbH **FRACTAL: A Distributed System for Cognitive Edge Computing** (English, 45 min)	Espen Tallaksen - EmLogic AS **Making a structured VHDL testbench – for beginners** (English, 90 min)
	Patrick Urban - Cologne Chip AG **GateMate FPGA Bitstream Encryption** (English, 45 min)			Brian Colgan - Microchip Technology GmbH **Introduction to Vector Processing and Neural Network Acceleration on Microchip FPGAs** (English, 45 min)	
3:45 - 4:30 pm	**Coffee break**				
4:30 pm - 6:00 pm	Prof. Dirk Koch - Heidelberg University - ZITI **How to crash 100+ AWS FPGA instances and how to insert Trojans into bitstreams** (English, 45 min)	Timo Osterkamp - Sokratel Kommunikations- und Datensysteme GmbH **Easy workflow to run MATLAB Simulink Models on Xilinx Zynq UltraScale+ hardware** (English, 45 min)	Benoit Pradelle - AMD Xilinx **Doing more with HLS before synthesis: code analyzer and other new features in Vitis HLS** (English, 45 min)	Harald Werner - Efinix Inc. **Real Low power, high speed Devices from Efinix** (English, 45 min)	Espen Tallaksen - EmLogic AS **Making an medium advanced testbench using verification components and high-level transactions, with a focus on ensuring proper Specification Coverage** (English, 90 min)
	Sven Hager - Synogate UG **Demonstration Setup for HashCache** (English, 45 min)	Ansgar Hein - SGET **Maximizing Efficiency: The Importance of FPGA Standardization** (English, 45 min)	Alexander Flick - PLC2 GmbH **Acceleration Kernels – Efficient Development with the HLS Design Methodology** (English, 45 min)	Joachim Müller - Efinix Inc. **Taking TinyML to the next Level – Efinix Sapphire RISC-V Core with Enhanced AI support** (English, 45 min)	
6:00 - 6:30 pm	**Lucky Draw**				
from 6:30 pm	**Workshop SGET e.V., everyone who is interested in FPGA Standardization is invited to join the working group**				

	Thursday - July 6			
	Safety & Security	**Architecture**	**Board Level**	**AI/ML**
09:00 am - 10:30 am	Jens Michaelsen & Martin Kellermann - Avnet EMG GmbH, Microchip Technology **Functional Safety in FPGA Designs** (English, 45 min)	Mark Frost - Intel **Protecting your FPGA Intellectual Property** (English, 45 min)	Kamil Rudnicki - Brightelligence sp. z o.o. **Do FPGA designers and hardware designers need to talk? A practical approach to shortening the project timeline** (English, 45 min)	Jens Stapelfeldt - AMD Xilinx **Pervasive AI Update from AMD** (English, 90 min)
	Patrice Brossard + Ugur Konuk - Future Electronics **FPGA security solutions overview** (English, 45 min)	Karl Wachswender - Lattice Semiconductor Corporation **European Cyber Resilience Act and its Impact on IEC 62443 and Embedded Industrial System Security** (English, 45 min)	Dirk van den Heuvel - Topic Embedded Systems **How your FPGA design decisions affect PCB board performance** (English, 45 min)	
10:30 - 11:00 am	**Coffee break**			
11:00 am - 12:30 am	Baruch Mitsengendler - The MathWorks GmbH **Tackling Functional Safety challenges in FPGA, ASIC and SoC Design** (English, 45 min)	Oren Hollander - HandsOn Training **Agilex SoC Architecure** (English, 45 min)	Andreas Wolf - Avnet-Silica **Exploring Avnet's low-cost AMD-Xilinx MPSoC Development Kit, the ZUBoard 1CG** (English, 45 min)	Stanislaw Klinke - EBV Elektronik GmbH & Co. KG **Boost your AI applications utilizing a top performing AI Processor for Edge Devices along with FPGA** (English, 45 min)
	Florian Pramme & Dr. Christian Siemers - Ostfalia - University of applied sciences **Mastering functional safety designs with high level synthesis** (English, 45 mn)	Anton Kuzmin - ARIES Embedded GmbH **How to embrace your fears and succeed in a project with SoC-FPGA. Designing with PolarFire-SoC.** (English, 45 min)	Dr. Dmitry Eliseev - RWTH Aachen University **Turning your FPGA into a fast multi-channel ADC** (English, 45 min)	Bill Jenkins - Achronix Semiconductor Corporation **Conversational AI on Achronix FPGAs** (English, 45 min)
12:30 - 1:30 pm	**Lunch break**			
1:30 pm - 3:00 pm	Burkhard Jour - PQShield **The new Post-Quantum cryptography standards from NIST: what do you need to know?** (English, 45 min)	Ernst Wehlage - PLC2 GmbH **Kria SOM Vision – How to add the Video Coder** (English, 90 min)	Alexander Wirthmueller - MPSI Technologies GmbH **PCIe, MIPI CSI-2, HDMI and DDR memory across platforms from an Open Source perspective** (English, 90 min)	Alexander Flick - PLC2 GmbH **Versal ACAP: Principles of AI Engine based Accelerators** (English, 45 min)
	Martin Kellermann & Perttu Saarela - Microchip Technology GmbH **Post-Quantum Protection on Intelligent Edge SoCs** (English, 45 min)			Dimitri Hamidi - The MathWorks GmbH **An Integrated Workflow for Deploying Deep Neural Networks on FPGAs** (Englisch, 45 Min)
3:00 - 3:30 pm	**Coffee break**			
3:30 pm - 5:00 pm	Tim Fernandez-Hart - Sundance Multiprocessor Technology Ltd **Secure Video Streaming Using Dedicated Hardware** (English, 45 min)	Oren Hollander - HandsOn Training **Direct RF FPGAs: The Next Generation for RF Applications** (English, 45 min)	Dimitri Hamidi - The MathWorks GmbH **Making the most of FPGAs for Power Electronics Development** (English, 45 min)	Angelo LoCicero / Gerhard Nedok - Intel & Arrow Central Europe GmbH **Intel Ai Suite IP - Unleash the potential of Agilex DSP Blocks** (English, 45 min)
	Lionel Rivière - eShard | Solutions for Cybersecurity **Hardware attacks on FPGA: An overview of threats and security mechanisms** (English, 45 min)	Myrtle Shah - Heidelberg University - ZITI **Yosys & nextpnr – open flows for commercial use cases** (English, 45 min)	Holger Krumme - HTV Halbleiter-Test & Vertriebs-GmbH **Buyer beware - detecting counterfeit components!** (English, 45 min)	Valerio Tenace - Rapid Silicon Inc. **An HDL-Aware Pair Programmer from the Future** (English, 45 min)
5:00 - 5:30 pm	**Lucky Draw**			