Circuit Synthesis with VHDL

Seminar

Applicable Technologies	Requirements	Contact
All Xilinx® FPGAs including SoCs	Basic understanding of digital circuit technology Basic understanding of concepts of any programming or scripting language	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de
Fee (net per person)	**Inclusive**	**Duration**
SE Free of charge	Training material Beverages during breaks Lunch	1 day

Workshop

The course »Circuit Synthesis with VHDL« is part of a free series of PLC2 seminars for beginners.

Programmable logic devices, such as FPGAs, have been established in all areas of our daily life. They are used in mobile phones, IoT devices, automobiles, and data centers. The areas of application are as diverse as their size. They serve as protocol adapters, signal converters, or accelerators to analyse video, radar, and sensor data. VHDL is a powerful hardware description language which meets all requirements to design a digital circuit of this scale. Various abstraction mechanisms enable the developer to create such designs quickly and effectively. VHDL already eliminates various programming errors during the design. Typically, VHDL is used at the Register Transfer Level (RTL) to design digital circuits of any complexity. Furthermore, VHDL can be used to integrate larger subcircuits on the system level. In addition to the VHDL language constructs for synthesis, the language offers various functionalities to describe complex verification models. Hence, it is possible to verify digital circuits from a simple gate to the System on Chip (SoC) in advance.

In this seminar, selected aspects of the hardware description language VHDL, based on the language revision IEEE Std. 1076-2008, will be covered.

Agenda

01. Inroduction to VHDL
    - History and future of VHDL
    - Language concept
    - Hardware modelling techniques
    - Design flow

02. Hardware description with VHDL
    - Entity/architecture
    - Package
    - Library/context

03. Language elements
    - Signals, variables, constants
    - Processes and concurrency
    - Control structures
    - Functions/procedures
    - Generic descriptions

04. VHDL types
    - Predefined types and operators
    - User-defined types
    - Attributes