PLC2 DSP

Professional DSP Design Using Vitis Model Composer

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
Xilinx® FPGAs, Zynq® SoCs and MPSoCs, Versal® ACAP	Basic understanding of digital signal processing Basic experience with the MATLAB® software	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 2,800	Training material	5 days
PW € 3,250	Plus beverages during breaks Lunch	5 days

Workshop

This five-days workshop includes teaching DSP and acceleration development methods for both generic FPGAs and Versal® ACAP technologies using the Xilinx® Vitis™ Tools Model Composer, which needs to be used with MATLAB® and Simulink®.

Different toolboxes are provided with Vitis™ Model Composer: HDL Toolbox, HLS toolbox, and AIE toolbox. DSP algorithms can be implemented in different ways or in a combination with these methods. Hardware developers in particular benefit from the HDL toolbox, image processing is best supported in particular by the HLS toolbox and the AI Engine kernels can in turn be optimally developed with the AIE toolbox with Versal®.

Processor-supported hardware acceleration methods are also simplified with these methods.

The workshop is recommended for algorithm developers, hardware developers and software developers.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. **Introduction to a model based DSP design**

02. **Model Composer optimized block library**

03. **Data types and conversion**
    - Creating custom blocks in Vitis™ Model Composer
    - Implementing DSP functions using Vitis™ Model Composer

04. **Digital filter design and implementation**
    - Utilizing design implementation tools
    - Transforming algorithmic specifications

05. **System control**

06. **Verification methods**
    - Optimization methodologies using Vitis™ Model Composer

07. **Vivado® ML integration**
    - Creating Versal® AI Engine graphs and kernels
    - Connecting AI Engine blocks and non-AI Engine blocks
    - Verifying and debugging AI Engine code using the Vitis™ analyzer
    - Simulating and debugging using AI Engine library blocks

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