PLC2 DSP

Compact DSP Design for FPGAs Using Vitis Model Composer

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® FPGAs, Zynq® SoCs and MPSoCs	Basic understanding of digital signal processing Basic experience with the MATLAB® software	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

With MATLAB® and Simulink®, Vitis™ Model Composer offers several toolboxes for DSP development. The HDL Toolbox is based on VHDL/Verilog code generation and the HLS toolbox the C/C++-based code generation using Vitis™ HLS. The methods of the DSP-based design model are explained and applied in accompanying exercises with data type management, MATLAB® simulation, HDL-simulation, and C-simulation, and code generation that offers resource and performance optimizations much more easily than the classic VHDL/Verilog design draft.

Model-based abstraction facilitates faster design drafts, simulation is performed under MATLAB®, and optimization is simplified with Xilinx-optimized toolboxes and MATLAB® libraries enabling system simulations incorporating the DSP algorithms implemented for the Xilinx® platform.
The capabilities of a flexible data type management with integer, fixed point, or floating point and with support of quantization and necessarily conversion will be described and demonstrated.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. MATLAB® and Simulink® basics
- Introduction to a model-based DSP design

02. Vitis™ Model Composer explained
- Model composer optimized block library
- Data types and conversion

03. Digital filter design
- FIR design
- Serial/Parallel filter
- Filter implementation

04. Verification
- Simulink® simulation
- HDL and co-simulation

05. System control
- H/W over sampling
- Block operations

06. Vivado® ML integration
- Vitis™ and Vivado®
- Model composer integration
- Clock management

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