Vivado Design Suite Tool Flow

Online Live

Workshop

Applicable Technologies	Requirements	Contact
7 Series FPGAs and newer devices	Basic knowledge in VHDL or Verilog Basic knowledge in digital design techniques	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 600	Training material	1 day
WO € 800	Plus beverages during breaks Lunch	1 day

Workshop

The Vivado® Design Suite is a new and highly integrated design environment explicitly created for handling huge, system-oriented programmable designs. The main pillars are a unified and scalable database allowing great cross-probing possibilities and a unique test environment for a shortened learning curve. In addition, increased adherence to industry standards such as AMBA® AXI4, IP-XACT (for metadata for self-developed IP cells), Tool Command Language (Tcl), Synopsys Design Constraints (SDC) etc. allows for easy scalability and simplified automation of the development process.

Vivado® is conceptually designed in a way to deal with all aspects (logic, SW, I/O, mixed-signal, etc.) of programmable technology and this is for designs of the complexity of up to 100M ASIC gates.

This is an introductory class. It teaches planning techniques and strategies as well as different software functions. The class guides the attendee through a complete design flow: Starting with the specification of the functionality, passing through synthesis, verification, and implementation to the final test in hardware.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Project planning
    - Overview
    - Specifications and design documents
    - Technology selection
    - Verification

02. Vivado® IDE overview and projects
    - Vivado® tool features and benefits
    - Creating new projects and modifiying projects
    - RTL elaboration
    - Simulating the design
    - Synthesis and implementation
    - Configuration

03. Vivado® tool flow
    - Overview
    - Synthesis and reports
    - Implementation and reports
    - Vivado® IDE projects
    - Scripted design flow

04. I/O planning and clock constraints
    - Overview
    - Using the I/O planner view
    - Entering clock constraints

05. Vivado® simulator (XSIM)
    - Overview
    - HDL testbenches
    - Simulating a design

VIVADO

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