Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints

Online Live

Workshop

Applicable Technologies	Requirements	Contact
7 Series and UltraScale™ FPGAs	Knowledge of FPGA technology, Vivado® software flow and basic constraining Working experience with VHDL or Verilog Solid knowledge of digital design techniques.	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

The Vivado® design suite is a new and highly integrated design environment explicitly created for handling huge, system-oriented programmable designs.

The main pillars are a unified and scalable database allowing great cross-probing possibilities and a unique test environment for a shortened learning curve. In addition, increased adherence to industry standards such as AMBA® AXI4, IP-XACT (for metadata for self-developed IP cells), Tool command Language (Tcl), Synopsys Design Constraints (SDC), etc. allows easy scalability and simplified automation of the development process. Vivado® is conceptually designed in a way to deal with all aspects (logic, SW, I/O, mixed-signal, etc.) of programmable technology and this is for designs of a complexity of up to 100M ASIC gates.

This class gives a detailed discussion of the creation of XDC (Xilinx® Design Constraints) and the static timing analysis. On top, proper usage of FPGA resources is discussed along with how the unified Vivado® design database can be used efficiently for e.g., analysis purposes.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Review of essentials of FPGA
02. FPGA design techniques
03. Accessing the design database
04. Static timing analysis and clocks
    - Setup checks and clocks
    - Timing reports
    - Hold checks
05. Inputs and outputs
    - Creating input delays
    - Creating output delays
06. Timing exceptions
    - Multicycle paths
    - False paths
    - Max/min delay exceptions
07. FPGA design methodology
    - Device and system architecture
08. HDL coding techniques
09. Reset methodology
10. Synchronization circuits and the clock interaction report
    - Single bit synchronization circuits
    - Bus synchronization circuits
    - Clocks and synchronizers
11. Timing closure
    - Baselining
    - Isolating common timing bottlenecks
    - Last mile strategies
12. FPGA design
13. Methodology case study

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