PLC2 Tools & Methodology

Professional Vivado

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
7 Series FPGAs, UltraScale™, UltraScale+™	Working experience with VHDL or Verilog Solid knowledge of digital design techniques and FPGA technology	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 2,800	Training material	5 days
PW € 3,250	Plus beverages during breaks Lunch	5 days

Workshop

The Vivado™ design suite is a new and highly integrated design environment explicitly created for handling huge, system-oriented programmable designs.

The main pillars are a unified and scalable database allowing great cross-probing possibilities and a unique test environment for a shortened learning curve. In addition, increased adherence to industry standards such as AMBA® AXI4, IP-XACT (for metadata for self-developed IP cells), Tool command Language (Tcl), Synopsys® Design Constraints (SDC) etc. allows for easy scalability and simplified automation of the development process. Vivado™ is conceptually designed in a way to deal with all aspects (logic, software, I/O, mixed signal, etc.) of programmable technology and this is for designs of a complexity of up to 100M ASIC gates.

This class gives a thorough introduction to this new development environment, reaching from the first steps through more advanced techniques to constrain with XDC (Xilinx® Design Constraints – based on SDC) and the associated timing analysis.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. FPGA design methodology summary
02. Introduction to the Vivado™ design suite
03. Vivado™ design flows
04. Visualization for analysis designing with IP
    - Working with IP/IP integrator
05. Basic timing constraints and reports
    - Basic timing constraints
    - Basic static timing analysis
06. Accessing the design database
07. Static timing analysis and clocks
    - Setup checks and clocks
    - Timing reports
    - Hold checks
    - Multiple clocks
08. Input and output constraints
09. Timing exceptions
    - Multicycle paths
    - False paths
    - Max/min delay exceptions
10. Advanced timing analysis
11. Advanced I/O interface constraints
    - Single data rate vs. double data rate
    - System-synchronous interfaces
    - Source-synchronous interfaces
12. Project-based and non-project flows
13. Scripting using project based and non-project batch flows
14. FPGA design methodology
15. HDL coding techniques
16. Reset methodology
17. Synchronization circuits and the clock interaction report
18. Timing closure
19. FPGA design methodology case study

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