Professional FPGA Circuit Design Technique

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
All Xilinx® FPGAs incl. SoCs	None	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 2,800	Training material	5 days
PW € 3,250	Plus beverages during breaks Lunch	5 days

Workshop

The workshop on digital circuit design techniques – especially for FPGA technology – is the foundation for many courses in our training catalog. The general introduction discusses basic circuit elements of an FPGA. This comprises combinational and sequential circuits, such as multiplexers, lookup-tables, flip flops, RAMs, adders, multipliers, clock generators, and I/Os. Subsequently, more complex circuits like comparators, counters, shift registers, FIFOs, and Finite State Machines (FSM) are composed of base elements. The knowledge gained in this way can now be transferred to the Xilinx® UltraScale+™ technology.
In order to create a wider theoretical and practical groundwork, profound knowledge of clock networks, reset distribution as well as »asynchronous vs. synchronous« is conveyed. This also includes designs with multiple clock networks, data exchange, and synchronization between clock domains (Clock Domain Crossing – CDC). In addition, several synchronization circuits are going to be examined. The challenges of synchronous circuit design are not limited to the design in the FPGA.

Another chapter of this course is dedicated to the problems and solutions of digital inputs and outputs, as well as the timing relation between data paths and clock distributions in a system consisting of several digital devices. Key points are the understanding of propagation delays just as setup and hold times. In the final chapter of this training, data exchange protocols for coupling basic circuits and IP cores are discussed. This involves classic off-chip protocols such as UART, SPI, and I²C; similarly address and streaming-based on-chip protocols such as AXI4, AXI4-Lite, AXI-Stream.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Generic FPGA architecture
- Primitive elements in an FPGA
- Internal wiring and switching-matrices
- Dedicated arithmetic blocks and memory
- I/O resources und clock networks
- Integrated IP blocks
- SoC (processors, FPGA area, peripherals)

02. Basic circuits
- Flip flop, register, shift-register
- Adder, counter
- RAM, ROM
- FIFO
- Finite state machine

03. Xilinx® UltraScale+™ technology
- Logic and arithmetic resources
- Wiring and clock networks (incl. clock buffers and PLLs)
- Memory and I/O resources
- Integrated IP blocks

04. Codes and protocols
- One-hot code, Johnson-code, Grey-code
- Manchester encoding, 8b/10b, 128b/130b
- Streaming protocols
- Address-based protocols

05. Clock domain crossing
- Metastability
- Synchronization circuits

06. Design patterns/best practices
- Design optimization
- Coding rules

07. Inputs/outputs
- System vs. source synchronous interfaces
- SDR vs. DDR interfaces

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