Easy Start FPGA Vivado

Online Live

Easy Start

Applicable Technologies	Requirements	Contact
FPGA technologies	None	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
ES € 1,900	Plus Xilinx® evaluation board with example solutions Beverages during breaks Lunch	2 days

Workshop

The workshop »Easy Start FPGA Vivado« covers the basic approach to the FPGA development cycle. It teaches the participant everything that is necessary to get started. In this workshop, the Xilinx® design tool Vivado® will be used.
After a short introduction to the FPGA design techniques and the process of development, this class concentrates on synthesis/simulation, circuit implementation, and startup of the FPGAs. Special emphasis is placed on working on FPGA projects. For a successful implementation, the designer needs a fundamental understanding of FPGA-specific design techniques, appropriate functional inference using VHDL, and the associated verification. Furthermore, a basic understanding of the target technology is required. These topics are covered by this workshop. During the course of this class different design tasks, regularly found in the real world, are presented along with their solutions. Functionality as intended gets proven through simulation and by testing in real hardware (evaluation board).

A more thorough knowledge transfer is available through the PLC2 Power Workshop »Professional FPGA«.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. **Introduction to the FPGA development process**
    - Design entry
    - Simulation
    - Synthesis
    - Implementation
    - Configuration

02. **FPGA design techniques**
    - Combinatorial circuits
    - Clocked circuits
    - Asynchronous/synchronous circuits
    - Implementation of clocking structures
    - Design guidelines

03. **VHDL synthesis**
    - VHDL language concept
    - VHDL processes
    - Infering combinatorial circuits
    - Infering clocked circuits

04. **Internal clocking structures with DCM/PLLs**
    - Clock networks

05. **Clock Management MMCM**
    - MMCM modes

06. **Control engines implemented as finite state machines**
    - Overview of FSM types
    - Coding of FSMs

07. **VHDL simulation**
    - VHDL testbench concept
    - VHDL timing model
    - Generating stimulus

08. **Implementation of internal data storage**
    - Declaration of multidimensional arrays
    - Coding style
    - Creation of storage elements using Core generator