Dynamic Function eXchange (DFX)

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® FPGAs, SoC, MPSoC, RFSoC, Versal®	Basic knowledge of FPGA technology and in VHDL or Verilog Basic knowledge of the Vivado® design flow	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

This course demonstrates how to use the Vivado® design suite to construct, implement, and download a Partially reconfigurable (PR) FPGA design.
You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow.

This course covers both the tool flow and mechanics of successfully creating a PR design. It also describes several techniques focusing on appropriate coding styles for a PR system, as well as system-level design considerations and practical applications. The PR design approach allows strategies for non-realtime multiplexing hardware functions by exchanging partial bitstream configuration files. This is an advanced methodology for in-system programming FPGA devices.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Partial reconfiguration overview
02. Partial reconfiguration tool flow
03. Partial reconfiguration bitstreams
04. Managing timing for partial reconfiguration
05. Partial reconfiguration in embedded systems
06. Dynamic function eXchange in Vitis™
07. Debugging partial reconfiguration designs
08. Partial reconfiguration design recommendations
09. PCIe core inclusion with partial reconfiguration