PLC2 Tools & Methodology

Designing with the Xilinx Analog Mixed Signal Solution

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® 7 series FPGAs	Basic knowledge in VHDL Knowledge of Xilinx® FPGAs Knowledge of Xilinx® design tool flow	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

Processing Analog Mixed Signals (AMS) in an FPGA is already feasible today! This course is an introduction to the analog mixed-signal design solution with Xilinx® FPGAs and their associated tools and techniques.

This class' target audience is analog and digital hardware engineers, interested in using different AMS techniques. This course mainly takes advantage of the Xilinx® Analog to Digital Converter (XADC) core. The complete front-to-back design flow is covered. This includes the generation of test signals, binding the different digital processing components, and in particular the analysis of the XADC block.
Using a Xilinx® evaluation board with an FMC add-on card, accompanying exercises assure the different possibilities to be applied practically.
This starts with the simulation of an analog input signal and finishes with a digital analysis of that stimulus in the FPGA design like with e.g., an FFT.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. AMS overview
02. ADCs and DACs theory
03. Xilinx® XADC architecture
04. AMS design flow
05. LabVIEW design environment
06. XADC debug and monitor
07. HDL design flow
08. Embedded design flow
09. Vivado® design flow