Debugging Techniques Using the Vivado Logic Analyzer

Online Live

Workshop

Applicable Technologies	Requirements	Contact
7 Series FPGAs and newer technologies	Basic knowledge of Xilinx® FPGAs Basic knowledge in VHDL	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

The former ChipScope Pro tool is now fully integrated in the Vivado® tool suite. This provides the possibility of FPGA internal logic analysis along with different configurations of the trigger unit and data storage options, to ideally fit the requirements of the measurement task. Even HDL novices may take advantage of this alternative verification mechanism. It may complement (or replace extensively) HDL simulations when bringing new systems into service.

During the exercises, the debug cores get created for real designs based on a provided evaluation board. The attendee learns how the software of the logic analyzer is structured and in which way commonly-known functions, such as the trigger menu and waveform representation of the captured data, are available. This tool is of particular interest for embedded controller applications. Additionally, this verification method allows accelerating of HDL based simulations through the possibility of probing data in hardware and exporting the results for file I/O usage during the next simulation. This class shows all the important features necessary to master even demanding FPGA verification scenarios.

The attendees of the F2F course will be provided with exercises alongside an evaluation board.

Agenda

01. The hardware debug methodology and how it works
02. Inserting the debug cores
03. Instantiating the debug cores
04. Debug flow in IP integrator
05. Triggering and storage
06. Visualizing data – the analyzer tool tips and tricks
07. Time for timing
08. Optimization – area groups
09. Case studies
10. Scripting remote access
11. The Vivado® serial I/O analyzer

Exercises

01. Inserting a debug core from the Vivado® Design Suite
02. Adding a debug core using the HDL instantiation flow
03. Debugging flow – IPI block design
04. Tips and tricks
05. VIO TCL scripting
06. Remote access