PLC2 Tools & Methodology

Compact Vitis for Acceleration

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Architecture: Xilinx® Alveo™ accelerator cards, SoCs, and ACAPs	Basic knowledge of Xilinx® FPGA architecture Comfort with the C/C++ programming language, software development flow	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

Sequential processing or data path speed is a bottleneck in many high-end systems based on CPUs, whereas FPGAs provide massive parallel data processing along with an optimized data path. A system with CPU and FPGA combination would be an ideal solution by utilizing the best of both worlds. But FPGA development is more complex and often hard to achieve time to market requirements. Xilinx® developed a hard- and software-based ecosystem to utilize FPGAs as an application-specific processing element along with CPUs. Xilinx®'s unified software environment Vitis™ offers the capabilities to translate CPU functions into such FPGA mappings using HLS or to generate native RTL-based kernels. With these techniques, FPGA-based development is streamlined by staying in high-level programming languages and using defined APIs for application offloading and data path acceleration.
In this course, you will learn how to develop, debug and profile new or existing C/C++ and RTL applications with Vitis™ targeting both Data Center (DC) and Edge-embedded applications. Beyond the kernel generation concepts, it will be derived how to run designs on the Xilinx® Alveo™ accelerator board or Edge development kits. The course is focused on building a software application using an OpenCL or native C API to deploy the Linux-based Xilinx® Runtime (XRT) to efficiently accelerate specific functions in kernels and control data movement on an embedded processor or PCIe®-based x86 platforms.

This course adds on top of the »Vitis HLS« course and leverages basic tool flow experience from the compact series workshops on embedded development.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Introduction to the Vitis™ unified software platform
02. Vitis™ IDE tool overview
03. Vitis™ command line flow
04. Introduction to hardware acceleration
05. Processing offload vs. path optimization
06. Vitis™ execution model and XRT
07. OpenCL framework fundamentals
08. Xilinx® OpenCL synchronization techniques
09. XRT native C API
10. Profiling and debugging
11. Introduction to C/C++ based kernels
12. Using the RTL kernel wizard to reuse existing IP as accelerators
13. Optimization methodology
14. C/C++ based kernel optimization
15. Host code optimization
16. Optimizing the performance of the design
17. Vitis™ accelerated libraries
18. DMA data flow IPs

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