PLC2 Tools & Methodology

Compact FPGA Circuit Design Technique

Online Live

Workshop

Applicable Technologies	Requirements	Contact
All FPGA technologies	None	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

The workshop on digital circuit design technique – especially for FPGA technology – is the foundation for many courses in our training catalog.

The general introduction to »Compact FPGA Circuit Design Technique« discusses the basic circuit elements of an FPGA. This comprises combinational and sequential circuits such as multiplexers, lookup tables, flip-flops, RAMs, adders, multipliers, clock generators, and I/Os. Subsequently, more complex circuits like comparators, counters, shift registers, FIFOs and Finite State Machines (FSM) are composed of base elements. The knowledge gained in this way can now be transferred to the Xilinx® UltraScale+™ technology. In order to create a wider theoretical and practical groundwork, additional topics are clock networks, reset distribution as well as asynchronous vs. synchronous circuits. This also includes designs with multiple clock networks, data exchange, and synchronization between clock domains (Clock Domain Crossing – CDC).

The challenges of synchronous circuit design aren't limited to the design in the FPGA only. Another chapter of this course is dedicated to the problems and solutions of digital inputs and outputs, as well as the timing relation between data paths and clock distributions in a system consisting of several digital devices. Key points are the understanding of propagation delays just as setup and hold times.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Generic FPGA architecture
    - Primitive elements in an FPGA
    - Internal wiring and switching matrices
    - Dedicated arithmetic blocks and memory
    - I/O resources und clock networks
    - Integrated IP blocks
    - SoC (processors, FPGA area, peripherals)

02. Basic circuits
    - Flip-flop, register, shift-register
    - Adder, counter
    - RAM, ROM
    - FIFO
    - Finite state machine

03. Xilinx® UltraScale+™
    - Logic and arithmetic resources
    - Wiring and clock networks (incl. clock buffers and PLLs) memory and I/O resources
    - Integrated IP blocks (e.g. MGT, PCIe)

04. Codes and protocols
    - One-hot code, Johnson-Code, Grey-Code
    - Manchester Encoding, 8b/10b, 128b/130b
    - Streaming protocols