PLC2 Embedded

Professional Versal ACAP

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Versal® ACAP series	Knowledge of digital systems Basic insight into Xilinx® Vivado® design flows Basic understanding of Xilinx® FPGA architecture and HDL principles	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 2,800	Training material	5 days
PW € 3,250	Plus beverages during breaks Lunch	5 days

Workshop

This Power Workshop combines the content of the PLC2 Workshops »Compact Versal ACAP for the Hardware Designer« and »Compact Versal ACAP for the Software Designer«.

In this course, you will gain the necessary in-depth knowledge of architecture and the workflow for designing with the Versal® ACAP technology and the related toolchains. For the hardware developer the Vivado® IP integrator and Vivado® are most relevant, whereas the software developer will focus on the Vitis™ software development platform which provides a wide range of tools and methods for an efficient deployment of the heterogeneous ACAP device architecture. All the same, in today's complex projects both experts need to share their domain knowledge. Thus, the tool-specific and architecture related aspects for both, hardware and software development are covered in this course.
Also, the system-level architecture requires strategies for a successful design that takes the partitioning of the full design into account. This guides the mapping of certain functions to a particular ACAP hardware feature to scale the design according to requirements. It will be shown how tools provided for analysis, debugging and deployment on hardware can help to understand the actual design result.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Overview of embedded hardware development
02. Versal® ACAP architecture introduction
03. Scalar engines, adaptable and intelligent engines
04. Driving the IP integrator tool
05. NoC and memory introduction and concepts
06. Clocks, resets, and I/O connectivity
07. Driving the Vitis™ software development tools
08. Creating custom peripherals based on AXI
09. Versal® programming interfaces
10. Design tool flow summary
11. Versal® ACAP processing system
12. Versal® application partitioning
13. Application development and debugging
14. Operating system support
15. Versal® ACAP software build flow: PetaLinux and Yocto
16. Software stack for Versal® ACAP
17. System simulation
18. Versal® platform management controller
19. Boot and configuration
20. Introduction to system integration and validation methodology
21. Outlook on acceleration toolflow

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