

# Expert Zynq-7000 SoC

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Zynq®-7000 SoC	Basic knowledge of the programming languages VHDL, C and the Zynq®-7000 SoC architecture	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de
Fee (net per person)	Inclusive	Duration
<b>OL</b> € 2,800	Training material	5 days
<b>PW</b> € 3,250	Plus beverages during breaks Lunch	5 days

## Workshop

The Power Workshop »Expert Zynq-7000 SoC« builds on the Power Workshop »Professional Zynq-7000 SoC«. This allows the attendees to deepen and extend their knowledge of Zynq®-7000 SoC architecture.

This course discusses in particular the handling of the specific tools provided by Vivado® and Vitis™. Additionally, several important peripheral components available as part of the processor system (PS) will be explained in more detail. Furthermore, the usage of the processor cores in Zynq®-7000 devices is discussed in more depth. The configuration possibilities of a DMA constitute another major topic. During this five day’s class, the contents are further reinforced by the means of various exercises.

There are both embedded hardware issues in the Vivado® tool flow and embedded software deals with issues in which participants already should demonstrate knowledge.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

## Agenda

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| 01. Embedded systems development review                  | 11. Software boot and PL configuration                          |
| 02. Zynq®-7000 SoC processing system overview            | 12. HDL system simulation with an embedded processor            |
| 03. Debugging using the ChipScope pro analyzer           | 13. Advanced boot methodology and boot details                  |
| 04. JTAG to AXI master debug IP transactions             | 14. Advanced Cortex®-A9 processor services                      |
| 05. Block RAM memory controllers                         | 15. Advanced DMA controller configuration on the Zynq®-7000 SoC |
| 06. External memory controllers for static memory        | 16. High-speed peripheral configuration on the Zynq®-7000 SoC   |
| 07. Memory controllers for dynamic RAM                   | 17. Low-speed peripherals on the Zynq®-7000 SoC                 |
| 08. AXI streaming interface                              | 18. Ethernet support using LwIP stack                           |
| 09. System data movement: low latency and high bandwidth |   |
| 10. Advanced processor configurations                    |   |