PLC2 Embedded

Expert Versal ACAP AI Engine

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Versal® ACAP series	Basic knowledge of embedded controller and Vitis™ tool flow Basic knowledge of the programming language C/C++	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 2,800	Training material	5 days
PW € 3,250	Plus beverages during breaks Lunch	5 days

Workshop

With the Versal® Adaptive Compute Acceleration Platform (ACAP) family, Xilinx® offers devices with a special IP, the AI Engine. The AI Engine offers high-performance and low latency capabilities for advanced data processing. This course shows the application acceleration with C/C++ kernels on Versal® AI Engine.
The workshop introduces the Versal® AI Engine processing element with its internal VLIW processing unit and the supporting interfaces. These yield connections to data paths and memory hierarchy in the grid of the AIE tiles. Such features enable an efficient data flow for processing tasks at hand.
With the Vitis™ unified development platform, the AI Engine is set up to run acceleration functions written in C/C++ code. Understanding the basic kernel programming, the advanced data flow graph API is presented to connect multiple of such kernels.
These data flow graphs are deployed in the system-level design flow in Vitis™. This methodology also covers data movement between compute domains, i.e., within the AI Engine and towards NoC and PL, and utilizes the different interface types and connection capabilities.
The advanced features to interface these graph elements effectively, such as streams, cascade stream, buffer location constraints, run-time parameterization, and respective APIs are explained and can be experienced in hands-on lab exercises, where hints are given to optimize such designs.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Overview of Versal® ACAP architecture
02. Introduction to the Versal® AI Engine architecture
03. Versal® AI Engine memory and data movement
04. Versal® AI Engine tool flow with Vitis™
05. Application partitioning on Versal® ACAP
06. Data types: scalar and vector data types
07. AI Engine API and intrinsic functions
08. Window and streaming data APIs
09. The programming model: single kernel
10. The adaptive data flow graph
11. Advanced graph input specifications
12. The programming model: multiple kernels
13. Application partitioning walkthrough
14. System design flow with Vitis™
15. Introduction to debugging with AI Engine kernels
16. AI Engine application debug and trace
17. Overview of AI Engine kernel optimization
18. Advanced intrinsic functions
19. Versal® AI Engine DSP library overview

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