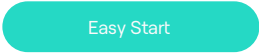


Easy Start Embedded for Zynq UltraScale+ MPSoC Systems



| Applicable Technologies | Requirements | Contact |
|----------------------------------|---|--|
| Xilinx® Zynq® UltraScale+™ MPSoC | Basic knowledge of embedded controller, FPGA technology, and the programming languages VHDL and C | Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de |
| Fee (net per person) | Inclusive | Duration |
| ES € 1,700 | Training material Beverages during breaks Lunch | 2 days |

Workshop

This workshop introduces the FPGA designer into the world of embedded designs based on the proven Zynq® UltraScale+™ MPSoC technology. This class teaches the attendee how embedded systems can be created and customized with Zynq® UltraScale+™ MPSoC devices and introduces the principles of embedded software development on the available CPUs.

family and the Vitis™ unified development platform. During these two days, each attendee will carry out all important steps of the development phase: generation of the hardware, incrementally extend hardware functionality, create and bind software libraries to create executable applications. All required concepts are trained in lab sessions and verified on an evaluation board.

Along with the introduction of the device family features, the attendee learns the methodology to implement an embedded application on the Zynq® UltraScale+™ MPSoC architecture. Emphasis is placed on the project planning of embedded designs taking advantage of the Zynq® UltraScale+™ MPSoC

A more detailed coverage is available in the PLC2 Power Workshop »Professional Zynq UltraScale+ MPSoC«, or the three-day courses »Compact Zynq UltraScale+ MPSoC for the Hardware Designer« and »Compact Zynq UltraScale+ MPSoC for the Software Designer«.

Agenda

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|---|--|
| <ul style="list-style-type: none"> 01. Zynq® UltraScale+™ MPSoC architecture basics 02. Overview of embedded hardware development 03. Overview of embedded software development 04. Designing a custom AXI peripheral 05. Standalone software platform development 06. Interrupts – hardware and software support | <ul style="list-style-type: none"> 07. Software debugging with Vitis™ 08. Zynq® UltraScale+™ MPSoC boot and configuration <p>Exercises</p> <ul style="list-style-type: none"> 01. Exploring the architecture of the Zynq® UltraScale+™ MPSoC 02. Driving the IP integrator tool 03. Driving the Vitis™ toolchain 04. Building a custom AXI IP 05. Application development 06. ZU+ MPSoC interrupts 07. Application debugging 08. ZU+ MPSoC boot and configuration |
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