PLC2 Embedded

Compact Zynq UltraScale+ MPSoC for the Hardware Designer

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Zynq® UltraScale+™ MPSoC and RFSoC	Basic knowledge of digital system architecture Basic knowledge in VHDL or Verilog language and C/C++ is an advantage	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

This 3-day course provides both the tool- and architecture-specific aspects necessary for development with the Xilinx® Zynq® UltraScale+™ MPSoC device. At the beginning, special attention will be paid to the Embedded Design Flow.
The course focuses on embedded hardware development with the Xilinx® Vivado® tool using the IP Integrator, which also covers software development with the Xilinx® Vitis™ tool.
Then the overall architecture of the Zynq® UltraScale+™ MPSoC Processing System (PS) is discussed. For the connection of AXI-based IPs in the Programmable Logic (PL) to the Processing System (PS) it is essential to understand the AXI protocol as well as the Interrupt structures.
The final section of this course consists of creating and verifying custom IP cores with an AXI based interface port to the Processing System.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Embedded UltraFast™ design methodology
02. Embedded hardware development
03. Driving the IP integrator tool
04. Driving the Vitis™ tools
05. Zynq® UltraScale+™ MPSoC architecture
06. Cache coherency management
07. System protection and isolation
08. Introduction to AXI
09. Hardware aspects of interrupts
10. Adding and connecting AXI IP
11. Creating custom AXI IPs
12. Bus functional model simulation

ZYNQ UltraSCALE+

AMD XILINX Authorized Training Provider