PLC2 Embedded

Compact Zynq-7000 SoC for the Hardware Designer

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Zynq®-7000 SoC	Knowledge in VHDL and FPGA technology Basic knowledge of the programming language C	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

This workshop focuses on the creation of hardware platforms for the established Zynq®-7000 SoC technologies, as well as the handling of the supporting Xilinx® Vivado® design suite.

From the start, it serves to introduce the system designer to the basic architectural elements of the Zynq®-7000 SoC devices. On one hand, the Processor System (PS) will be covered. The different building blocks are introduced and discussed in detail along with their configuration possibilities. On the other hand, the Programmable Logic (PL) and the AXI interface to the processor system are explained. Another major topic is dedicated to the creation and simulation of streamlined AXI4-based peripheral components. Moreover, interrupt handling in basic software projects with the Vitis™ unified development platform is introduced and practical handling of the interactive operation of the target chip is experienced.

To focus on the software development tool (Vitis™), please refer to the workshop »Compact Zynq-7000 SoC for the Software Designer«, which is the follow-up course to this one.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Embedded design overview
02. IP integrator and the PS configuration wizard
03. Software development using Vitis™
04. Introduction to AXI
05. Interrupts
06. Adding hardware to an embedded system
07. Cortex®-A9 processor basics
08. Designing a custom AXI peripheral
09. Using the create and package IP wizard to build a custom AXI peripheral
10. Bus functional model simulation

ZYNQ

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