PLC2 Embedded

Advanced Zynq UltraScale+ MPSoC for the Hardware Designer

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Zynq® UltraScale+™ MPSoC and RFSoC	Basic knowledge of digital system architectures Basic knowledge in VHDL or Verilog language and C/C ++ is an advantage	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

This 3-day course provides both the tool- and architecture-specific aspects necessary for development with the Xilinx® Zynq® UltraScale+™ MPSoC device.

The focus of this course is on embedded hardware development with the Xilinx® Vivado® tool using the IP-Integrator, including software development using the Vitis™ tool. The overall architecture of the Zynq® UltraScale+™ MPSoC Processing System (PS) is discussed in detail to understand the architecture in the silicon processing system that interfaces to the Programmable Logic (PL). The APU includes the Arm® Cortex®-A53 cores, the RPU includes the Cortex®-R5F cores, and the PMU includes a MicroBlaze™ system.

And it will be necessary to protect and isolate accesses in a system of shared peripherals and memory if MPSoC-based designs are running simultaneously. For this connection of AXI-based IPs in the Programmable Logic (PL) to the Processing System (PS), it is essential to understand the AXI protocol with features like coherency management and virtual system management. The final section of this course includes platform management, power management, and inter-processor-interrupt concepts.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. The Arm® APU: Cortex®-A53 processor
02. The Arm® RPU: Cortex®-R5F processor
03. The Zynq® MPSoC system architecture
04. 64-bit and 32-bit architecture features
05. Cache coherency management
06. Hypervisors introduction
07. Virtualization hardware support
08. On-chip memories and its architecture
09. Boot configuration and boot image creation
10. System memory management
11. Peripheral and memory protection
12. Zynq® UltraScale+™ MPSoC clocking and PS resets
13. AXI variations and transactions
14. The Platform Management Unit (PMU)
15. Power management using the PMU
16. Inter Processor Interrupts (IPI)

ZYNQ UltraSCALE+

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