PLC2 Embedded

Advanced Versal ACAP AI Engine

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Versal® ACAP series	Basic knowledge of embedded controller and Vitis™ tool flow Basic knowledge the programming language C/C++	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

With the Versal® Adaptive Compute Acceleration Platform (ACAP) family, Xilinx® offers devices with a special IP, the AI Engine. The AI Engine offers high-performance, low latency capabilities for advanced data processing. This course enables algorithm programmers to deploy C/C++ kernels on Versal® AI Engines.

The workshop introduces the Versal® AI Engine processing element with its internal VLIW processing unit and the supporting interfaces. These yield connects to data paths and memory hierarchy in the grid of the AI Engine tiles. Such features enable an efficient data flow for processing tasks at hand. For the implementation of discrete AI Engine kernels, attendees will be using the Vitis™ unified development environment, where the AI Engine is set up to accelerate functions written in C/C++.

To gain insight into mapping complete signal processing chains, a tool flow is presented that uses data flow graphs to connect multiple kernels and shows the data movement in the Versal® AI Engine array. The system-level design flow with AI Engine-based kernels is covered to integrate an application utilizing the heterogenous Versal® ACAP architecture efficiently. To create such a heterogeneous system design, the data flow graph may route multiple compute domains such as PL and AI Engine.

The specific features to interface these graphs efficiently are explained and can be experienced in hands-on lab exercises. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Overview of Versal® ACAP architecture
02. Introduction to the Versal® AI Engine architecture
03. Basic Versal® AI Engine memory and data movement
04. Versal® AI Engine tool flow
05. Application partitioning on Versal® ACAPs
06. Data types and intrinsic functions window and streaming data APIs
07. The programming model: single kernel
08. The adaptive data flow graph
09. The programming model: multiple kernels
10. System design flow with Vitis™
11. Debug and profiling with AI Engine kernels
12. Versal® AI Engine DSP library overview

XILINX VERSAL

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