PLC2 DSP

# Vitis HLS

Online Live

Workshop

| Applicable Technologies | Requirements | Contact |
|---|---|---|
| Xilinx® FPGA, SoCs, MPSoCs, RFSoCs, and ACAPs | Knowledge of C language programming<br>Basic knowledge of FPGA architecture | Michael Schwarz<br>P. +49 7664 91313-15<br>E. info@plc2.de |

| Fee (net per person) | Inclusive | Duration |
|---|---|---|
| OL € 1,900 | Training material | 3 days |
| WO € 2,300 | Plus beverages during breaks<br>Lunch | 3 days |

## Workshop

Since the invention of FPGAs, the development methodology was continuously evolving from schematic entry towards RTL-based system modeling. A downside of these methods is the requirement to define the structure of the hardware, such as pipe lining, latency, data throughput, or area limitations along with the desired functional description.

HLS (High-Level Synthesis) methodology frees the embedded developer or algorithm developer to focus on the more abstract system modeling aspects without having to care about implementation-specific details of the hardware structure. Using C or C++ as a programming language, Vitis™ HLS automates the structural implementation and optimization by transforming the C-based model into synthesizable RTL.

This workshop trains on the HLS toolchain and introduces the approach of taking a C-based algorithm to derive a hardware IP component and quickly compare the results. Handling projects in labs starts with C-level verification for early detection of design errors and fast turn-around time. Further modules cover the control of the implementation flow to guide toward a desired IP structure optimized for speed, latency, or resources.
Integration of these IPs into a traditional FPGA design or acceleration-based applications is demonstrated to wrap up the training.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

## Agenda

01. Introduction to high-level synthesis

02. Using the Vitis™ HLS tool
    - Project creation in the Vitis™ HLS tool
    - C validation to IP creation

03. I/O interfaces
    - Block-Level I/O protocols
    - Port-Level I/O protocols

04. Pipelining for performance
    - Pipelining
    - Dataflow optimization

05. Optimizing structures for performance
    - Arrays in HLS
    - Array optimizations

06. Reducing latency
    - Improving latency
    - Loops: Impact on latency
    - Improving area
    - Controlling the resources used
    - Controlling the structure of the design

07. Introduction to the HLS design flow
    - RTL vs. C-based design

08. HLS vs. Vitis™ acceleration flow

09. Vitis™ HLS Tool: C coding rules and tips