

Designing with Ethernet MAC Controllers

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® FPGA, SoCs, MPSoCs, RFSocCs, and ACAPs	Basic knowledge of Xilinx® design tool flow Basic knowledge of FPGA technology and in VHDL	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de
Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

The Ethernet protocol is used in a variety of applications. Xilinx® offers various software and embedded hardware implementations for this, which require comprehensive knowledge for quick and effective use.

The two-day PLC2 course »Designing with Ethernet MAC Controllers« trains designers in the practical use of these Xilinx® specific Ethernet solutions. Starting with the basics of the Ethernet standard, the workshop covers protocol description and the OSI layer model. It describes the application of Xilinx® specific Ethernet solutions and reinforces this with exercises. Participants learn the hardware design and software development skills they need for successful implementation.

To complete the workshop, an example will be implemented and tested in real hardware communication with the computer using a Xilinx® FPGA evaluation board.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

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| <ul style="list-style-type: none"> 01. Ethernet basics 02. Network protocols 03. Ethernet frames 04. MAC: Media Access Control 05. Network protocols 06. Ethernet hardware 07. Physical layer 08. Ethernet interfaces 09. Flow control 10. Management interface | <ul style="list-style-type: none"> 11. Xilinx® EMAC solutions 12. 10/100 EMAC solutions 13. TEMAC 14. 10GE/25GE/40GE MAC 15. Integrated IP: 100G Ethernet MACs <p>Exercises</p> <ul style="list-style-type: none"> 01. Analyzing Ethernet frames 02. VLAN and Jumbo frames 03. Implementation 04. EMAC peripheral in loopback mode 05. TEMAC peripheral in loopback mode 06. Analyzing 10GE/25GE/40GE MAC frames |
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