Compact Versal ACAP: Power and Board Design

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Versal® ACAP	Familiarity with the Vivado® design suite Basic knowledge of circuit technology	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

With the powerful Versal® ACAP device family, the system level design requires an approach to create a power system that supports the device's engines for full capability.
This course provides the background to plan designs with these devices based on analysis of the design resource usage. AMD Xilinx® provides the tooling and guidance to successfully adopt such designs. The application of the PDM tool will be explained, and the lectures also describe the approaches to choosing a suitable package. Specific rules are provided for designing PL, PS, external memory, and transceiver interfaces. With these methods, a PCB design can be planned with respect to power supply, decoupling, and thermal management, which can be documented in the Versal® ACAP schematic checklist. You will learn to judge when signal integrity is important and relevant, to interpret, for example, IBIS models, and to select appropriate termination procedures. Signal refection and crosstalk effects are described and demonstrated by simulation based on UltraScale™ architecture examples. Furthermore, simulation examples are given for common memory interfaces as well as for serial transceiver interconnection.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Power solutions overview
02. Packaging and power integrity
03. Power design manager tool
04. Thermal solutions overview
05. Power management
06. Designing the power supply
07. Designing PL and interfaces
08. Designing memory and transceiver interfaces
09. Board system design guidance
10. Transmission lines
11. IBIS models and SI tools
12. Reflections and crosstalk
13. DDR4 / serial transceiver interface signal integrity analysis

Exercises:

01. Power estimation for Versal® ACAP
02. Versal® ACAP schematic checklist
03. Generating IBIS files
04. Designing transmission lines
05. Validating reflections and crosstalk
06. Validating DDR4 and transceiver interfaces

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