Compact Versal ACAP: PCI Express Systems

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Versal® ACAP	Knowledge of Vivado® design tool flow Basic knowledge of FPGA technology	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

This course introduces the features and capabilities of the PCIe® and Cache Coherent Interconnect blocks in the Versal® architecture. Learn how to implement a Versal® ACAP PCIe® solution in custom applications to improve time to market.
At the beginning of this class, an introduction to the vocabulary and the transmission protocol are given along with details on the structure and content of data packets. This is a solid foundation for building your own application. After that, the main aspects of this training class are simulation and implementation of a provided example design. This way, the learning experience is the most realistic while allowing one to easily put the theory into reality. The interface between the core blocks and the user application is especially emphasized. The available signals and their correct usage are discussed in the necessary detail. This course discusses both, the PL and the CPM PCIe® solutions.
During the training, the target technology will be the Versal® ACAP VCK190 evaluation board. The working principles and the protocol information, however, are equally valid for other Versal® hardware, too.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Introduction to PCIe®
02. Versal® ACAP - PCIe® solutions overview
03. PL PCIe® block architecture and functionality
04. PL PCIe® block interfaces overview
05. PL PCIe® block requester and completer interfaces
06. PL PCIe® block customization and simulation
07. PL PCIe® block implementation and debugging
08. PL PCIe® XDMA/Bridge subsystem
09. CPM block architecture and functionality
10. CPM block customization
11. CPM IP use cases

Exercises:

01. Defining PCIe® protocol transactions
02. Defining PCIe® transactions in descriptor format
03. Constructing the PCIe® block
04. Simulating the PCIe® block
05. Implementing the PCIe® block
06. Debugging the PCIe® block
07. Exploring XDMA
08. Designing CPM PCIe® DMA in IP integrator