Compact Versal ACAP: Connectivity

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Versal® ACAP	Familiarity with the Vivado® design suite Experience in Versal® ACAP serial transceiver Basic knowledge of circuit technology and usage of Windows-based tools	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

The Versal® Adaptive Compute Acceleration Platform (ACAP) allows very fast interfaces to external components based on significantly improved silicon structures as well as new IP Core configuration wizards. Realization challenges are shifting from chip level to board level with the new Versal® platform. Extreme accuracy in PCB design is mandatory to achieve high-speed data rates.
This workshop discusses in-depth designing for DDR4, PCIe® interfaces, and high-performance Ethernet MACs.
All design steps are described: IP configuration, functional simulation, and implementation. Designs will be demonstrated and verified on real Versal® hardware.

Additional focus is put on the physical layer – PCB design. Practical design and verification examples are discussed. Students learn how to apply design rules to the PCB design. Methodical tips and tricks are provided throughout the training.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Versal ACAP architecture overview

02. Cluster: memory interfacing
    - DDR4 memory enhancements
    - DDR memory controller architecture and functionality
    - DDRMC IP configuration
    - Design rules and practice
    - Realization of other memory interfaces

03. Cluster: PCIe®
    - PCIe® Gen3/Gen4/Gen5 enhancements
    - PL/CPM PCIe® blocks
    - PCIe® simulation and implementation
    - Debugging and PCB design

04. Cluster: integrated Ethernet MACs
    - MRMAC/DCMAC architecture and functionality
    - FEC options
    - Application examples

Exercises:
01. DDR4 interface design
02. PCIe® block customization and simulation
03. CPM block configuration
04. MRMAC design example