Compact UltraScale: High-Speed Memory Interfacing

Online Live

Workshop

Applicable Technologies	Requirements	Contact
All UltraScale™ FPGA/MPSoC/ RFSoC architectures	Knowledge of Vivado® design tool flow Basic knowledge of FPGA technology	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

This course targets to hardware designers, as well as to system architects and layout designers, who want to implement DDR4 interfaces in a system successfully.
The workshop starts with a comparison between DDR3 and DDR4 memories. The DDR4 enhancements are discussed together with the new features and operational details of DDR4 memories. All design steps are described: DDR4 design generation, functional simulation, and implementation. The design will be tested on real hardware. The special focus is on the physical layer – signal integrity. Parameters for signal quality and timing are covered. Practical design and verification examples are discussed. Simulation options on PCB level are described and demonstrated during exercises. The attendees will learn how to derive design rules for the PCB design. Methodical tips and tricks complete the content.

During the training, the target technology will be the Kintex® UltraScale™ FPGA KCU105 evaluation board.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Memory devices
02. Memory interface resources
03. Memory interface controller architecture and signals
04. MIG Wizard
05. DDR4 interface simulation
06. DDR4 interface implementation
07. DDR4 interface test and debugging
08. Board level design
09. PS memory controller
10. IBIS and SI tools
11. Memory interface PCB simulation

Exercises:

01. DDR4 IP customization
02. DDR4 IP simulation
03. DDR4 IP implementation
04. DDR4 IP debugging
05. Designing a PS memory interface
06. Memory interface PCB simulation