Compact UltraScale: Board Design and Signal Integrity

Online Live

Workshop

Applicable Technologies	Requirements	Contact
All UltraScale™ FPGA/MPSoC/ RFSoC architectures	Basic knowledge of FPGA technology	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

This course covers the board design of FPGA/SoC devices. The attendees will learn how to solve signal integrity problems with programmable devices. FPGA designers face new implementation possibilities and challenges.
This course discusses all steps for a successful board design: power supply, configuration, and interfacing. Solutions and challenges will be discussed for the pin definition. Moreover, rules for designing PCBs and handling thermal design will be commented on. You will learn to judge when signal integrity is important and relevant, to interpret, for example, IBIS models, and to select appropriate termination procedures. Signal refection and crosstalk effects are described and demonstrated by simulation based on UltraScale™ architecture examples. Furthermore, simulation examples are given for common memory interfaces as well as for serial transceiver interconnection.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. FPGA/SoC power supply
02. FPGA/SoC configuration and PCB
03. Signal interfacing
04. Architecture and packaging
05. PCB details
06. Thermal aspects
07. Tools for PCB planning and design
08. Transmission lines
09. IBIS models and SI tools
10. Reflections and crosstalk
11. DDR4 interface signal integrity analysis
12. Serial transceiver interface signal integrity analysis

Exercises:

01. Power estimation
02. Pin planning
03. Thermal design
04. Generating IBIS files
05. Designing transmission lines
06. Validating reflections and crosstalk
07. Validating DDR4 and transceiver interfaces

AMD XILINX Authorized Training Provider