PLC2 Connectivity

AXI Interface Technology

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® FPGAs, Zynq® SoC/ MPSoC/RFSoC, Versal® ACAP	Knowledge of the FPGA technology and the Xilinx® design tool flow Basic knowledge of VHDL	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

AXI is the de-facto standard for hardware interfacing IPs and processors with Arm® technologies and FPGA IPs as well.

This workshop teaches fundamental knowledge of this standard and the methods required, in order to write and verify your own standard conform hardware component or optimize the hardware system to achieve high data throughputs, low latencies or to achieve low resource utilization. Vivado® provides the IPs and tools and you will learn the methodologies to architect the hardware system.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. AMBA® - Arm® bus architecture
02. AXI4 and AXI variations
03. AXI transactions
04. AXI IP management
05. User IP creation
06. AXI IP verification
07. AXI performance analyzing
08. NoC in Versal® ACAP