PLC2 Connectivity

Compact UltraScale: Integrated PCI Express Systems

Online Live

Workshop

Applicable Technologies	Requirements	Contact
All UltraScale™ FPGA/MPSoC/ RFSoC architectures	Experience with PCIe® specification protocol Experience with Vivado® design environment	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,900	Training material	3 days
WO € 2,300	Plus beverages during breaks Lunch	3 days

Workshop

At the beginning of this class, an introduction to the vocabulary and the transmission protocol are given, along with details on the structure and content of data packets. This is a solid foundation for building your own application.
After that, the main aspects of this training class are simulation and implementation of a provided example design. This way, the learning experience is the most realistic while allowing one to easily put the theory into reality. The interface between the core block and the user application is especially emphasized. The available signals and their correct usage are discussed in the necessary detail. During the training, the target technology will be the Kintex® UltraScale™ FPGA KCU105 evaluation board.

The working principles and the protocol information, however, are equally valid for other technologies, too.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Introduction to the PCIe® architecture
02. Review of the PCIe® protocol
03. Connecting logic to the core
04. PCIe® block customization
05. Packet formatting details
06. Simulating a PCIe® system design
07. Endpoint application considerations
08. PCIe® in embedded systems
09. Application focus DMA
10. Design implementation
11. Root port applications
12. Debugging and compliance
13. Interrupts and error management

Exercises:

01. PCIe® block customization
02. PCIe® block IP simulation
03. PCIe® block IP implementation
04. Using the PCIe® Core in IP Integrator
05. Exploring Xilinx® DMA
06. Debugging the PCIe® design