PLC2 Architecture

Zynq UltraScale+ MPSoC for the System Architect

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Zynq® UltraScale+™ MPSoC and RFSoC	Conceptual understanding of embedded processing systems. C or C++ programming experience, including general debugging techniques	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

This course provides system architects with an overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family.

The emphasis is on leveraging the Arm® Cortex®-APU, RPU, and Platform Management Unit (PMU) capabilities. A separation of protected software tasks is needed when several OS are running in a system securely and safely.
A power-management concept in hard- and software will be demonstrated for getting higher reliability and optimized power consumption.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Zynq® UltraScale+™ MPSoC architecture overview
02. Hardware-software virtualization
03. QEMU for application development and debugging
04. Isolation for security and safety demands
05. Power management and platform mangement using the PMU
06. Caching and system coherency
07. DDR memory management and QoS
08. Booting concepts
09. Boot loading and boot images
10. Zynq® UltraScale+™ MPSoC ecosystem support