PLC2 Architecture

Zynq-7000 SoC for the System Architect

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Zynq®-7000 SoCs	Basic knowledge of embedded controller and FPGA technology Basic knowledge of Vitis™ unified platform and programming languages VHDL and C	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

This course teaches experienced system architects the knowledge necessary, in order to efficiently take advantage of the proven Zynq®-7000 SoC architecture.

The goal of this two-day class is to teach the benefits of the Zynq® architecture, so decisions can be taken easier while working on Zynq®-based projects. The architecture of the Arm® Cortex®-A9 processor-based processing system (PS) and the integration of the programmable logic (PL) are discussed. This allows system architects to use the Zynq®-7000 device successfully and efficiently. The topics of explanation are, amongst others the different building blocks of the processing system like I/O peripherals, timer, cache, DMA controller, interrupt handling, and the memory controller. In this context, the focus is put on efficient usage of the processing system's DDR controller from a PL point of view, interfacing between PS and PL, design techniques, and advantages of implementing functions in either the PS or PL. To gain more in-depth knowledge of the relevant development tools, please refer to the PLC2 Power Workshop »Professional Zynq-7000 SoC« or the three-day courses »Compact Zynq-7000 SoC for the Hardware Designer« or »Compact Zynq-7000 SoC for the Software Designer«.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Zynq®-7000 SoC overview
02. Inside the Application Processor Unit (APU)
03. Processor input/output peripherals
04. Introduction to AXI
05. Zynq®-7000 SoC PS-PL interface
06. Zynq®-7000 SoC booting
07. Using DMA on the Zynq®-7000 SoC
08. Memory resources and meeting performance goals
09. Zynq®-7000 SoC hardware design
10. Zynq®-7000 SoC software design
11. Debugging the Zynq®-7000 SoC
12. Zynq®-7000 SoC tools and reference designs

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