PLC2 Architecture

Versal ACAP for the System Architect

Online Live

Workshop

Applicable Technologies	Requirements	Contact
Xilinx® Versal® ACAP series	Basic knowledge in processor system architecture and Xilinx® FPGA architecture Basic knowledge of the programming language C/C++	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

With Versal® ACAP, Xilinx® offers a highly integrated technology, the adaptive compute acceleration platform. These Versal® chips have a heterogeneous architecture with multicore CPUs, programmable logic, PCIe connectivity, memory management, and AI Engines, which, in particular, provide compute-intense and DSP applications to be efficiently accelerated in hardware.

This workshop describes the ACAP architecture in order to foster insight into the optimal assignment of the building blocks for demanding tasks. Versal® offers a high-performant multiprocessor Arm® cluster as evolved from the Zynq® technologies and adds further hardened IPs beyond the programmable logic (PL) to support acceleration with various computation architectures. These are supported by a device-wide Network-on-Chip (NoC) to guarantee bandwidth within the device or to the attached memory controllers and help with timing closure in the design. This feature set is presented as a hardware platform. This concept is further supported by a full stack of software and hardware functions to allow focus on application development. The partitioning of the application will be derived to properly map tasks to the suitable Versal® features.

This approach to Versal® system designs is shown from platform generation to integration, adding simulation and debugging insights. The workshop is particularly suitable for system engineers and developers in the planning phase of complex applications.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Introduction to Versal® ACAP
02. ACAP architecture overview
03. ACAP adaptable engines (PL)
04. Processing system
05. PMC, boot, and configuration
06. IO connectivity
07. Clocking architecture
08. System interrupts
09. Timers, counters, RTC
10. Intelligent engines
11. NoC introduction and concepts
12. Device memory
13. Serial transceivers
14. Introduction to PCIe, CPM, and CCIX
15. Security features
16. System and solution planning – application partitioning
17. Hardware, IP, and platform development methodology
18. System integration and validation methodology

Exercises

01. Design tool flow
02. Boot and configuration
03. IO and clocking resources
04. Application development
05. NoC introduction system level simulation
06. Versal® ACAP platform creation

XILINX VERSAL

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