Professional FPGA

Online Live

Power Workshop

Applicable Technologies	Requirements	Contact
UltraScale/UltraScale+™ technologies	Basic knowledge in VHDL and digital technology is helpful Basic knowledge of Xilinx® Design tool flow	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 2,800	Training material	5 days
PW € 3,250	Plus beverages during breaks Lunch	5 days

Workshop

The PLC2 workshop »Professional FPGA« teaches the beginner or returning user how the building blocks of a Spartan®/Virtex® device work and in which way the available resources can optimally be used.
This class emphasizes the description of the fundamental architectural elements of the recent Spartan®/Virtex® FPGA technologies. After an initial overview, a detailed discussion of the different functional blocks such as for example the Configurable Logic Block (CLB), I/O-Block (IOB) for source- and system synchronous signal transmission in single or double data rate modes, DSP, etc.
Naturally, due to its special importance, the clock distribution system gets discussed in-depth.

Moreover, dedicated hardware blocks (e.g., GTP and PCIe®) get briefly discussed. Besides, adapted coding techniques are a topic, to get the most possible out of synthesis by using optimum coding for the target technology. The underlying instructions of the programming language VHDL as well as the standard proceeding for implementing a FPGA design are not topic of this workshop. Please refer to PLC2 workshops like »Compact VHDL for Synthesis«, »Compact VHDL for Simulation« or »Professional VHDL«.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. CLB architecture
    - CLB structure and routing
    - Slice resources
    - Distributed RAM/SRL
    - Using slice resources

02. Slice flip-flops
    - Control sets
    - Designing resets
    - Other reset considerations

03. Memory resources
    - Block RAM capabilities
    - FIFO capabilities
    - Using block RAM resources

04. DSP resources
    - DSP slice
    - Pre-Adder and dynamic pipeline control
    - Advantages
    - IP support and inference

05. I/O resources
    - SelectIO electrical resources
    - SelectIO logical resources
    - Power savings
    - Using SelectIO resources

06. Clocking resources
    - Clock networks and buffers
    - Clock management tile
    - Usage models
    - Using clock resources

07. Memory controller
    - Phaser and I/O FIFOs
    - Memory controller
    - Memory Interface Generator (MIG)

08. Dedicated hardware
    - Serial Gigabit transceivers
    - PCI Express® technology interface
    - System monitor

09. HDL coding techniques
    - Hierarchy
    - Control sets
    - Synthesis options

10. Timing constraints
    - Accessing the design database
    - Static timing analysis and clocks
    - Inputs and outputs
    - Timing exceptions

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