Compact UltraScale/UltraScale+

Online Live

Workshop

Applicable Technologies	Requirements	Contact
UltraScale/UltraScale+™ technologies	Basic knowledge in VHDL and digital design techniques Basic knowledge of Xilinx® Vivado® tool flow	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

This workshop teaches the first-time or recurring user in the way, the FPGA building blocks of the Xilinx® UltraScale/UltraScale+™ FPGAs work and how they can be used most effectively.
The emphasis of this workshop is put on the thorough discussion of the common architectural building blocks. After an overview, detailed explanations are given of the functional blocks such as e.g., configurable logic blocks (CLB), I/O blocks (IOB), DSP, etc. In addition to that, it will be explained how to migrate a 7 Series design to UltraScale™ architecture. Due to its crucial role in a FPGA design, special attention is given to the clocking resources and clock structure. To top the content off, dedicated hardware resources (such as e.g., GTX, GTY, and PCIe®) will briefly be introduced. Moreover, suitable coding techniques get explained throughout the class to allow synthesis to produce effective results based on the target device's resources. Exercises help to reinforce the learning process.
Neither hardware description languages like VHDL nor global implementation strategies are covered in this class. Please refer to PLC2 workshops like »Compact VHDL for Synthesis«, »Compact VHDL for Simulation« or »Professional VHDL«.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. Design migration software
    Recommendations
    Objectives

02. CLB architecture and HDL coding styles
    Configurable logic block
    HDL coding techniques

03. Clocking resources
    Resource layout and clocking structure
    Clock routing
    Clock buffers
    Clock management
    Using the clock resources

04. Memory and DSP resources
    Block RAM capabilities
    FIFO capabilities
    DSP capabilities
    Using RAM, FIFO, and DSP capabilities

05. I/O resources
    UltraScale™ architecture challenges and solutions
    I/O electrical and physical
    I/O logic and clocking
    SelectIO bank and pin names

06. FPGA design migration
    Objectives

07. Design migration case study
    Migration methodology
    XAUI design introduction
    Migrating the XAUI design case study

08. Transceiver overview
    Architecture improvements
    Transceiver wizard
    Transceiver usage