PLC2 Architecture

Compact FPGA 7 Series

Online Live

Workshop

Applicable Technologies	Requirements	Contact
7 series FPGA technologies	Basic knowledge in VHDL and digital design techniques Basic knowledge of Xilinx® Design tool flow	Michael Schwarz P. +49 7664 91313-15 E. info@plc2.de

Fee (net per person)	Inclusive	Duration
OL € 1,300	Training material	2 days
WO € 1,700	Plus beverages during breaks Lunch	2 days

Workshop

The PLC2 workshop »Compact FPGA 7 Series« teaches the first-time or recurring user the way, the FPGA building blocks of the 7 series devices of Xilinx® FPGAs work and how they can be used most effectively.
The emphasis of this workshop is put on the thorough discussion of the common architectural building blocks of the 7 series devices. After an overview, detailed explanations are given to the functional blocks such as e.g., Configurable Logic Blocks (CLB), I/O Blocks (IOB) for system- or source synchronous data transmission in single or double data rate mode, DSP, etc. Due to its crucial role in a FPGA design, special attention is given to the clocking resources and clock structure. Finally, dedicated hardware resources (such as e.g., GTP and PCIe®) will briefly be introduced.

Moreover, suitable coding techniques get explained throughout the class to allow synthesis to produce the best possible implementation results based on the target device's resources. Exercises help to reinforce the learning process.
Neither hardware description languages like VHDL nor global implementation strategies are covered in this class. Please refer to PLC2 workshops like »Compact VHDL for Synthesis«, »Compact VHDL for Simulation« or »Professional VHDL«.

Due to accompanying exercises, the course offers in-depth and practice-oriented training. Attendees of the online live course will do the practical exercises in the afternoon on their own.

Agenda

01. CLB architecture
- CLB structure and routing
- Slice resources
- Distributed RAM/SRL
- Using slice resources

02. Slice flip-flops
- Control sets
- Designing resets
- Other reset considerations

03. Memory resources
- Block RAM capabilities
- FIFO capabilities
- Using block RAM resources

04. DSP resources
- 7 Series FPGA DSP Slice
- Pre-Adder and dynamic pipeline control
- Advantages
- IP support and inference

05. I/O resources
- SelectIO electrical resources
- SelectIO logical resources
- Power savings
- Using SelectIO resources

06. Clocking resources
- Clock networks and buffers
- Clock management tile
- Usage models
- Using clock resources

07. Memory controller
- Phaser and I/O FIFOs
- Memory controller
- Memory Interface Generator (MIG)

08. Dedicated hardware
- Serial Gigabit transceivers
- PCI Express® technology interface
- XADC

09. HDL coding techniques
- Hierarchy
- Control sets
- Synthesis options

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